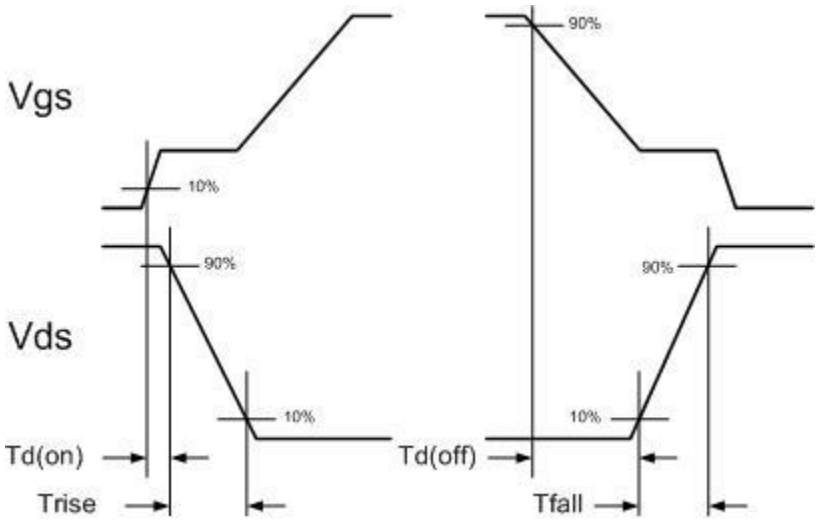
FTI-1000 MOSFET TMU

The MOSFET TMU option for the FTI-1000 consists of a module in a 2" x 7" x 9" box which connects to the FTI-1000 AC board in the test head. This module contains a conditioning board and a daughter board which provide all the signals required to measure the four basic MOSFET timing parameters. These are

- Td(on): The delay time to turn on.
- Td(off): The delay time to turn off.
- Trise: The time to turn fully on after the Td(on)
- Tfall: The time to turn fully after the Td(off)

The important parameters in programming a timing test are the VGS voltage and VDS voltage. Normally the timing is done from the 10% level of the VGS waveform for the turn on parameters, and from the 90% level of the VGS for the turn off parameters. (See diagram below, which shows the typical setup for an N channel device):

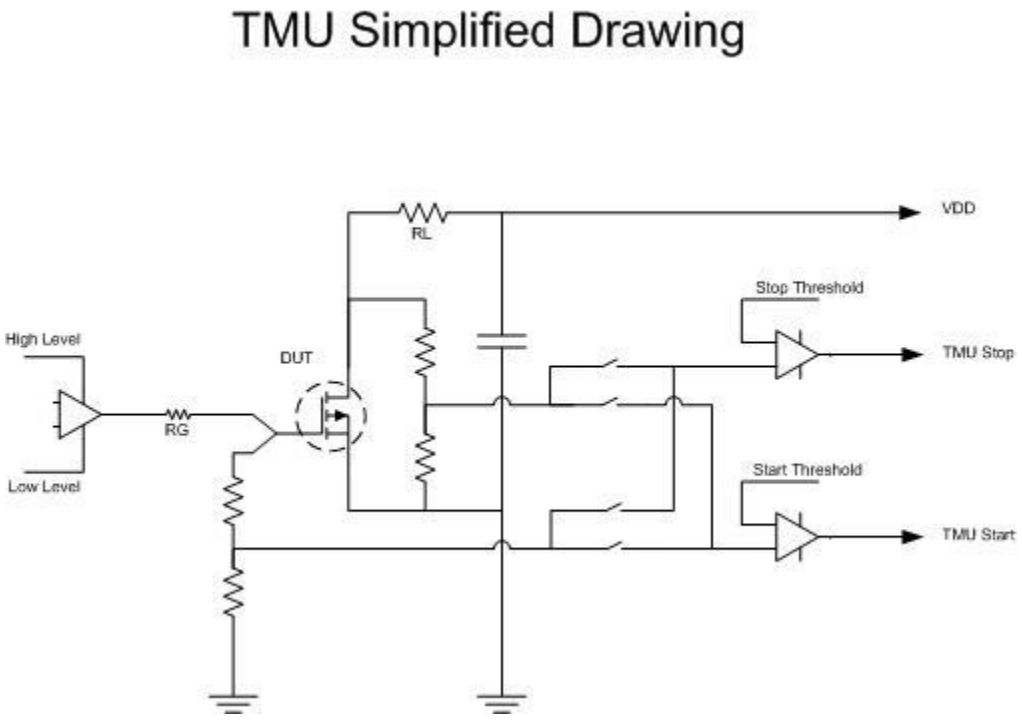


The thresholds in the above picture are shown at 10% and 90%, but these are programmable levels that are specified in the test function. As well as these thresholds, and the voltages, it is important to define the Drain current and the gate resistance. Both of these are specified in the device datasheet. Because the signals are so fast, and will be badly distorted by inductance, it is not possible to use a programmable resistance, or current limiter, so each different device type requires a specially made daughter board. This board has the gate driver and the series Rg resistor, as well as a capacitor to decouple the VDS, a load resistor RL, which along with the value of VDS will define the ID. Finally, this daughter board carries the attenuator to bring the high voltage drain signal down to a level that can be handled by the comparators on the TMU conditioning board.

The Timing.cs test function allows you to select just one parameter to be measured, or multiple parameters. Usually, one should select "All" and all 4 timing functions will be measured.

The TMU also has relays to allow it to be bypassed so that normal DC or AC parametric tests can also be done on the DUT. All of the normal MOSFET library functions can be used with the TMU, but because of the extra switching and stray capacitance, there may be a small degradation in performance of some AC tests, such as Rg, UIS and Qg.

The following is a simplified drawing of the TMU circuitry:

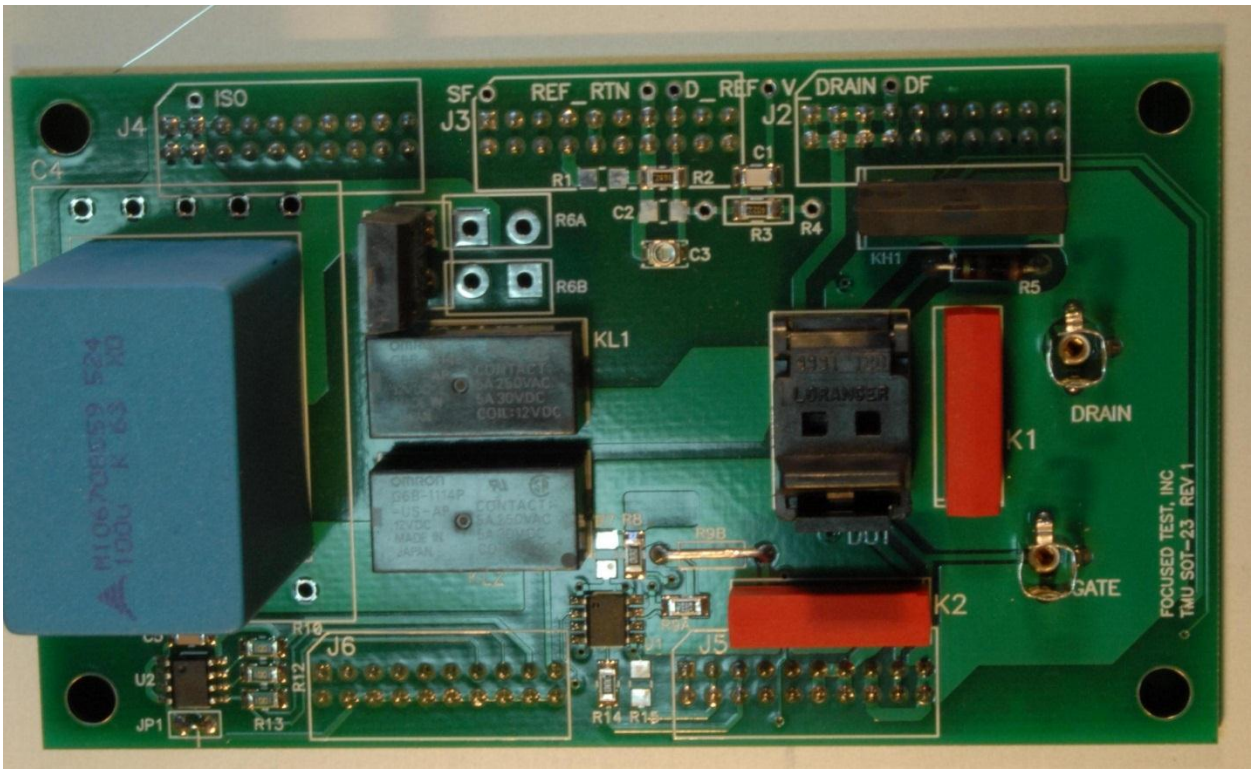


All of the description above has referred to N channel devices, but the TMU can also test P channel devices. It is just required to program the VGS and VDS to negative values, or to set the DeviceType in the properties of the flow to P_Channel.

There are two cables that connect the TMU to the test head. One is a 37 pin D shell cable, which has the power, control and the PECL timing signals going back to the tester. The second cable connects the DUT signals (DF, DS, SF, SS, GF, GS plus GND – need to attach to the test case).

The TMU cannot measure negative time, (and will return a zero reading) so it is important to make sure that the thresholds are set to appropriate levels. For example, in a Td(on) test, the gate will rise fast to the VGS(th), but then the Miller effect will hold the gate at this level until the device has fully turned on. This means that to get a valid reading, the VGS threshold must be set low enough to trigger before the VDS threshold is reached. Similarly, for a Trise test, the start threshold must be a higher voltage that the stop threshold.

Whenever possible (limited due to the size of the DUT socket), the Daughter board has two connectors that can be used to plug in scope probes to monitor the device signals. These test points are visible in the picture below on the right hand side.



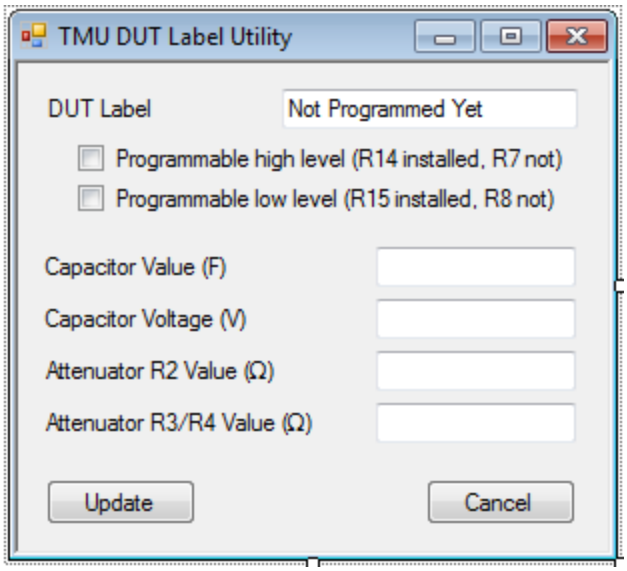
The daughter board must be present to do anything. When the program is first loaded, the TMU conditioning board and daughter board are both detected and the EEPROMs read. If the daughter board is changed without reloading the program, the cal factors will not be reloaded, and so results cannot be guaranteed.

Calibration:

The daughter board must be calibrated with the conditioning board. The function TMU3 in the FETACCalibrationLibrary6 does this. To run calibration, the DUT must be removed from the socket, and all cables must be plugged in. This calibrates the gate drive levels, the gate compare levels, the VDD capacitor charge rate, the Drain compare levels and the channel to channel skew.

There is a very simple diagnostic program TMU_Diag in the DiagnosticLibrary6. There is a parameter for DUT present or not, but for now, this is not used, and the diagnostic will only run correctly with an open socket.

If a daughter board is physically changed, before calibration or testing, the daughter board must first be programmed with TMU DUT Labeler tool. This will define the daughter board name, programmable level (for N or P channel devices), Capacitor size, Voltage, and attenuator values. See the below figure for the TMU DUT Label tool view.


TMU DUT Label Utility
DUT Label
Not Programmed Yet
Programmable high level (R14 installed, R7 not)
Programmable low level (R15 installed, R8 not)
Capacitor Value (F)
Capacitor Voltage (V)
Attenuator R2 Value (Ω)
Attenuator R3/R4 Value (Ω)
Update
Cancel