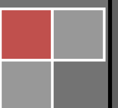
Focused Test Incorporated



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Revision

6.1 Working on unfinished sections.

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Introduction

Purpose of this Manual

The purpose of this manual is to provide information about the various libraries and tests that can potentially be run in FTI Studio, as well as information regarding the Instrument Configuration, Library Manager, and FTIMarker applications.

The first 2 chapters provide overviews regarding the FTI Studio interface and creating/running tests. Since they are only overviews, please consult the FTI Studio User Interface Manual for detailed and specific information regarding the interface and creating/running tests.

The majority of the remaining chapters are Library specific with the tests arranged in alphabetical order, grouped by Library. Chapter 3 deals with the FET DC library tests, chapter 4 the FET AC library tests, chapter 5 Math tests, chapter 6 FET AC Calibration tests.

The tests within each library chapter are arranged in alphabetical order and follow this format:

Overview: indicating what the general purpose of the test is,

Description: describes how the test performs and functions

Simplified Schematics/Block diagrams: presents a pictorial and conceptual overview of the functioning of the test

Test parameters: includes a screen capture of the test as well as testing parameters and values

Important Note:
Although the FTI 1000 system you purchased has the ability to run all the tests we provide, some of the tests are specific to the type of equipment you are using including any add on equipment. If your Focused Test representative has not covered or gone over with you specific tests that are to be run on your system(s), any excluded tests are not meant to be run and may result in run time errors.

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Chapter 1:
Working with FET DC Library Tests

Working with FET DC Library Tests

- ✓ BVDSS
- ✓ BVDSS_Ramp
- ✓ BVDSX
- ✓ BVGSO
- ✓ ConnectionTest
- ✓ Continuity
- ✓ DrainToDrainOpenShort
- ✓ DVSD
- ✓ DVSD_using_HPM
- ✓ Gate_Stress
- ✓ GFS
- ✓ GFS_DIGI
- ✓ GMP
- ✓ IDON
- ✓ IDSS
- ✓ IDSS_LV
- ✓ IDSS_UHV
- ✓ IDSX
- ✓ IGSS
- ✓ ISGS
- ✓ KELVIN
- ✓ LATCH
- ✓ OpenShort
- ✓ RDSON
- ✓ RDSON_Cal
- ✓ SingleEventBias
- ✓ SOA
- ✓ TRIP_TSN
- ✓ V_STATUS
- ✓ VDSON
- ✓ VDSON25mAmax
- ✓ VGD
- ✓ VGS
- ✓ VSD
- ✓ VTH
- ✓ VTH_Digi

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Libraries and Tests

Libraries in FTI are defined by the Library Manager application. This application contains a list of all the libraries and tests provided to FTI Studio. Depending on what components you are testing and what needs to be tested, you may not be able to run every single test. A run through of the Library Manager application and how to add additional tests is discussed later in the manual.

Important Note:

Although the FTI 1000 system you purchased has the ability to run all the tests we provide, some of the tests are specific to the type of equipment you are using including any add on equipment. If your Focused Test representative has not covered or gone over with you specific tests that are to be run on your system(s), any excluded tests are not meant to be run and may result in run time errors..

BVDSS Test

Overview:

Breakdown voltage or, BVDSS, is the voltage at which the reverse-biased body-drift diode breaks down and significant current starts to flow between the Source and Drain. Typically the Gate to Source voltage is set to 0 volts.

VDS voltages greater than the HV supply may be achieved with the addition of an external UHV (Ultra High Voltage) supply.

Description:

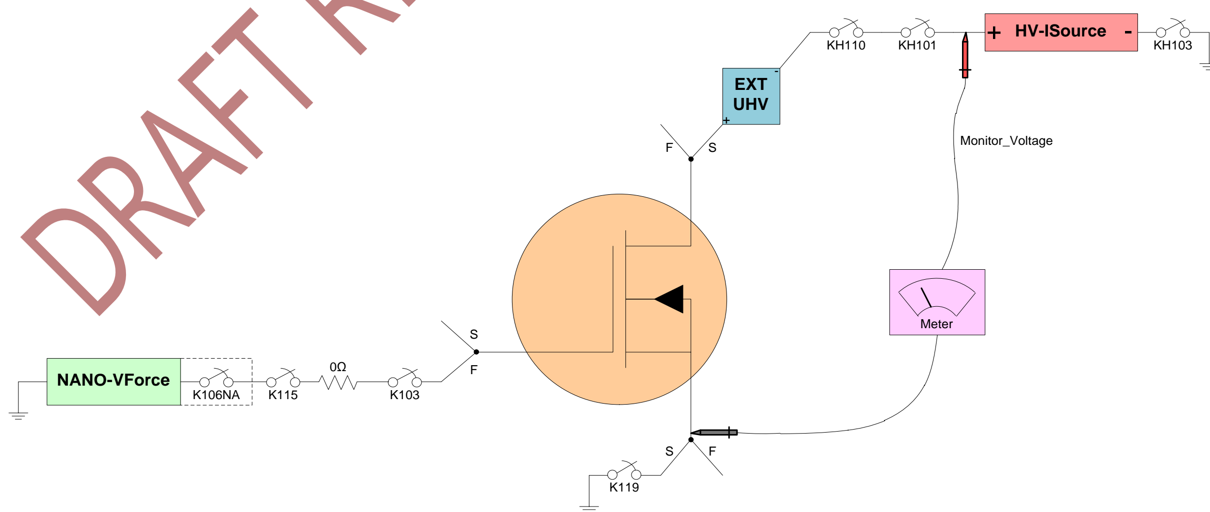
The Drain is connected to the HV supply. Gate is connected to the Nano VForce supply that can provide a gate voltage of up to +/- 25V.

The test runs by forcing a current (parameter *ID* is typically 250uA) into the Drain pin, forcing a Gate voltage (parameter *VGS*), and measuring the breakdown voltage (reported by the HV current supply to the measurement meter) that happens.

The *BVDSS_Max* limit is optional (use NaN or None if maximum limit is not desired), but there must be a minimum limit.

BVDSS Test Schematics

Configuration for N-Channel device, and optional EXT UHV boost supply.



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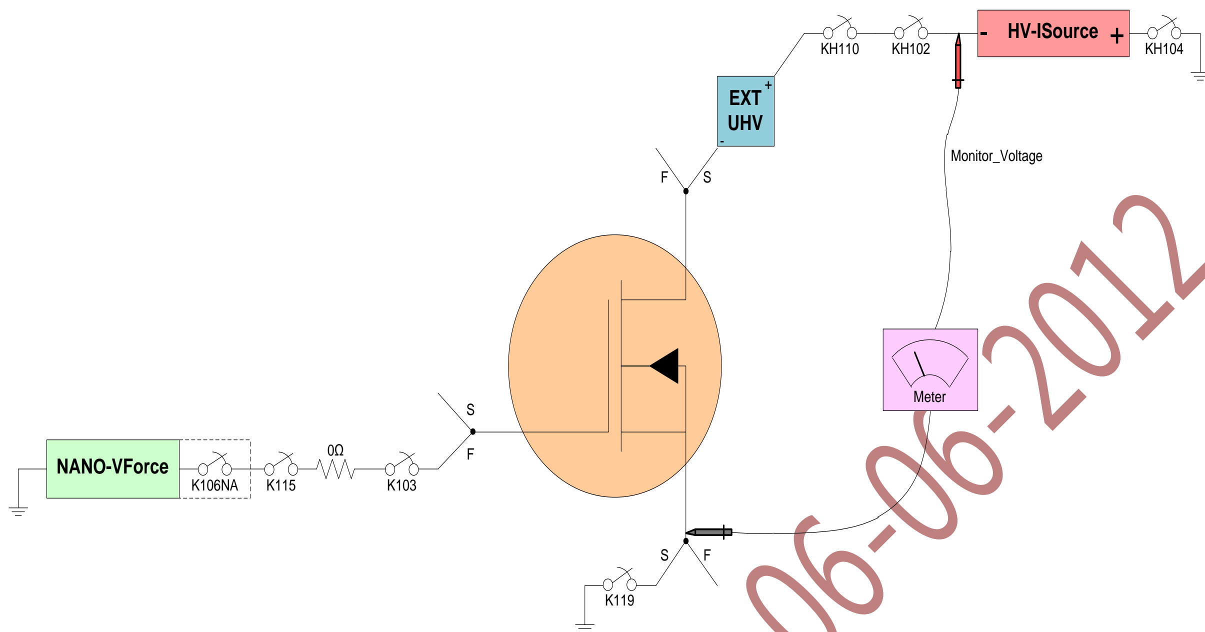
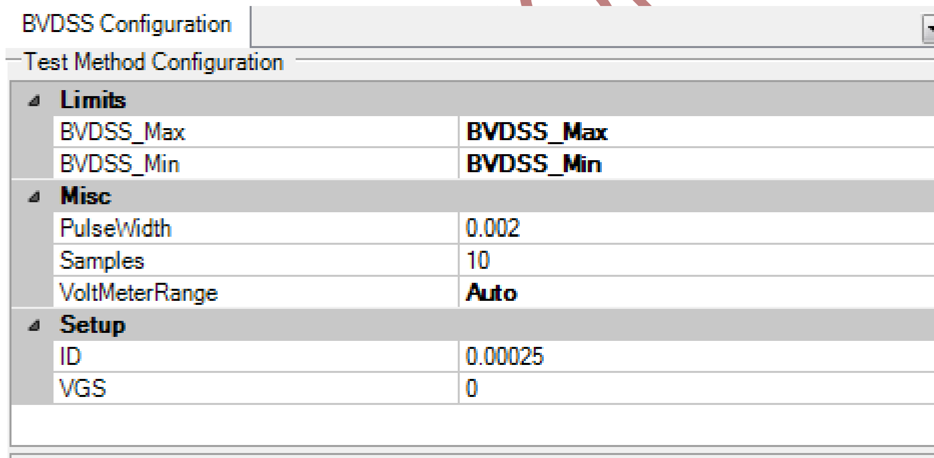
Configuration for P-Channel device, and optional EXT UHV boost supply.



BVDSS Test Parameters



BVDSS Configuration

Test Method Configuration

Limits	
BVDSS_Max	**BVDSS_Max**
BVDSS_Min	**BVDSS_Min**
Misc	
PulseWidth	0.002
Samples	10
VoltMeterRange	**Auto**
Setup	
ID	0.00025
VGS	0

BVDSS_Max ***BVDSS_Min***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. These values define the upper and lower limits of the break-down voltage result.
PulseWidth	Length of time, in seconds, to apply current. This must be set long enough for the power to rise fully. With

	longer cables, or coaxial cables going to a prober, extra time will need to be used, especially with higher voltage devices. Adjust the pulse (increase *PulseWidth*) until a stable reading is achieved.
Samples	Number of measurement samples to average result. (Sample rate is 11.6usec per sample. Ten (10) is normally adequate, but at lower currents, or with more noise, more samples may be required. If the number of samples is increased, *PulseWidth* may need to be increased to match. For example 100 samples would take 1.16msec, so with a *PulseWidth* of 2msec, this only allows 0.84 msec for the voltage to stabilize, which would be enough for low voltages, but above 100V this would probably mean that the voltage had not settled, and so the first few samples would skew the accuracy of the reading. If you try to reduce *PulseWidth* so that it is less than the time required to make the measurements, the software will generate an alarm each time the test runs. Measurement samples are taken at the end of the pulse.
VoltMeterRange	Provide means to force a voltage measurement range. Default automatically picks range based on *BVDSS_Max*. If *BVDSS_Max* is NaN or None, then range is determined by *BVDSS_Min* + 300. If the range is less than the break-down voltage, the reported voltage will be the maximum result provided by the range.
ID	Current to apply across Drain-Source.
VGS	Voltage to apply to Gate during break-down test.

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BVDSS_Ramp Test

Overview:

Breakdown voltage or, BVDSS, is the voltage at which the reverse-biased body-drift diode breaks down and significant current starts to flow between the Source and Drain. Typically the Gate to Source voltage is set to 0 volts.

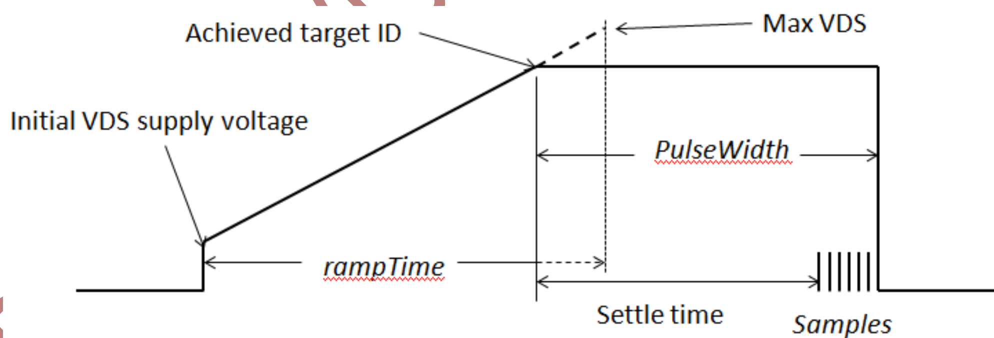
The purpose of the *BVDSS_Ramp* test is to slow down the rise edge of the VDS supply. Occasionally the combination of the DUT and VDS supply is not stable at break-down voltages. Slowing the rising edge of the VDS supply can sometimes eliminate, or reduce, the stability issues.

VDS voltages greater than the HV supply may be achieved with the addition of an external UHV (Ultra High Voltage) supply.

Description:

The Drain is connected to the HV supply. Gate is connected to the Nano VForce supply that can provide a gate voltage of up to +/- 25V.

The test runs by setting an initial VDS supply voltage, then ramp the voltage until the target *ID* is achieved, or until maximum VDS voltage is achieved. The voltage is held for the *PulseWidth* duration and voltage measurements taken.



The initial VDS supply voltage level is computed as 20% of the HV Max VDS voltage. If the UHV supply is also required, the initial VDS supply voltage will also include the UHV supply range setting.

The *Settle time* shown in the above diagram is computed from the *PulseWidth* minus the time for the measurement samples.

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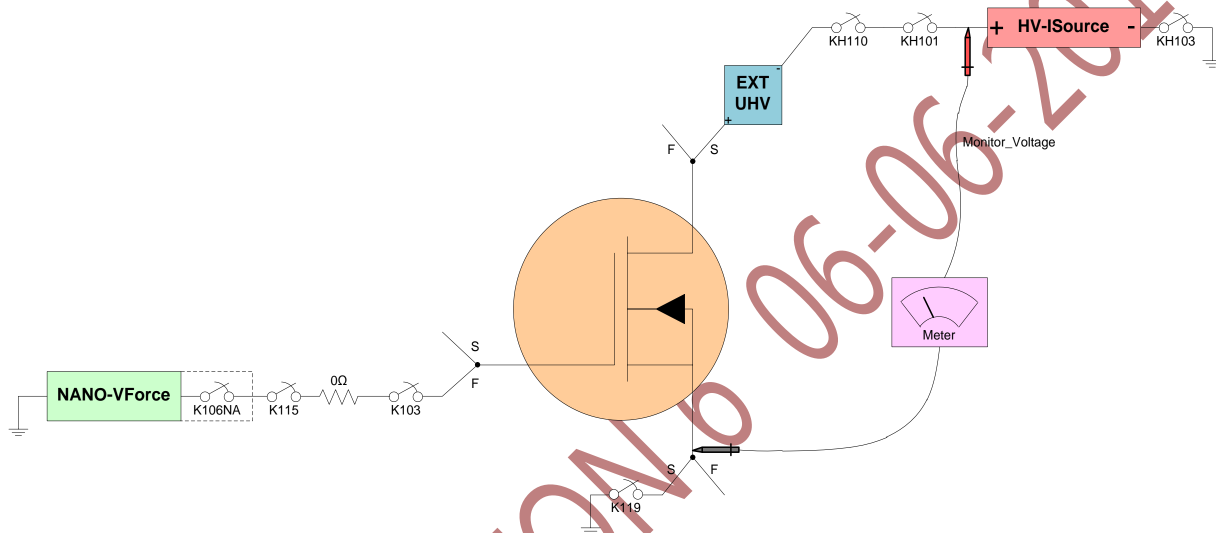
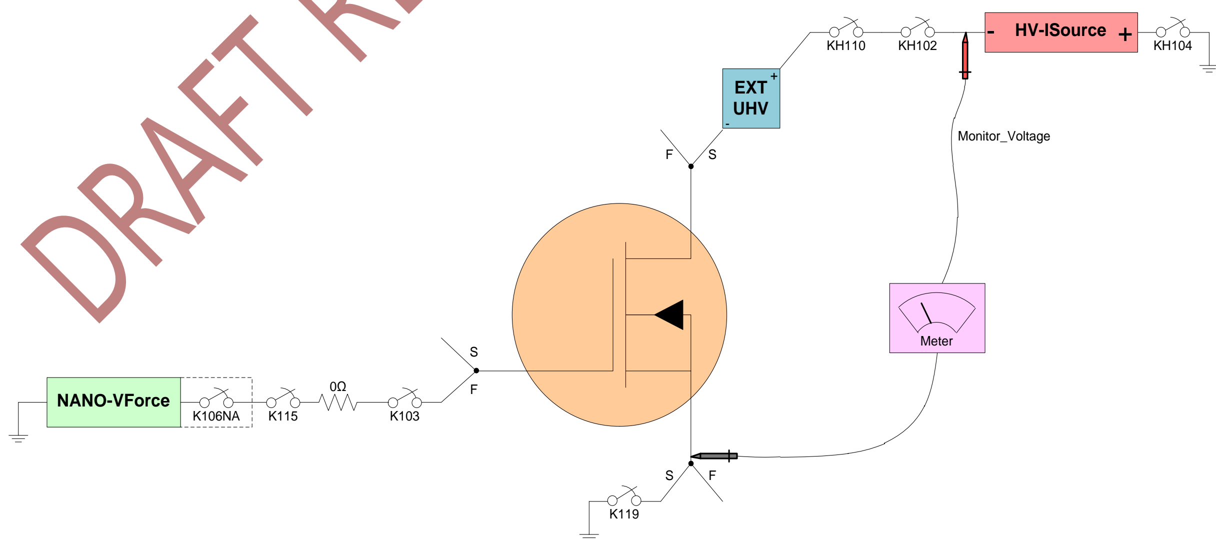
The maximum ramp VDS is either greater than the *BVDSS_Min* limit, or is the *MaxVDS* parameter value.

BVDSS_Ramp Test Schematics

Configuration for N-Channel device, and optional EXT UHV boost supply.



Configuration for P-Channel device, and optional EXT UHV boost supply.



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BVDSS_Ramp Test Parameters

BVDSS_Ramp Configuration

Test Method Configuration

Limits	
BVDSS_Min	**BVDSS_Min**
Misc	
displayIDSS	False
MaxVDS	0
PulseWidth	0.002
rampTime	0.002
Samples	10
Setup	
ID	0.00025
VGS	0

BVDSS_Min	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. This value defines the lower limit of the break-down voltage result.
displayIDSS	Set True to log additional measured ID value that caused ramp to terminate.
MaxVDS	Typically, the VDS value is derived from the *BVDSS_Min* limit. The *MaxVDS* parameter provides a means to override the derived value. **NOTE:** If this value is not 0, it should be greater than the *BVDSS_Min* limit. If MaxVDS is less than the *BVDSS_Min* limit, every test run will fail.
PulseWidth	Length of time, in seconds, to apply *VDS* voltage. This time does not include *rampTime*.
rampTime	Defines the maximum amount of time to ramp BVDSS supply until minimum target ID is achieved. This time does not include *PulseWidth* time.
Samples	Number of measurement samples to average measurement result after BVDSS supply has ramped to target *ID*.

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	Sample rate is 11.6usec per sample. Ten (10) is normally adequate, but at lower currents, or with more noise, more samples may be required. If the quantity of *Samples* is increased, *PulseWidth* may need to be increased to match. For example 100 samples would take 1.16msec, so with a *PulseWidth* value of 2msec, this only allows 0.84 msec between achieving *ID* condition to beginning of measurement samples.
ID	Target current to achieve across Drain-Source.
VGS	Voltage to apply to Gate during break-down test.

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BVDSX Test

Overview:

Breakdown voltage or, BVDSS, is the voltage at which the reverse-biased body-drift diode breaks down and significant current starts to flow between the Source and Drain. Typically the Gate to Source voltage will be 0 volts.

The *BVDSX* test will perform the break-down at a prior *VGS* test Gate voltage value times *VX* parameter value.

Description:

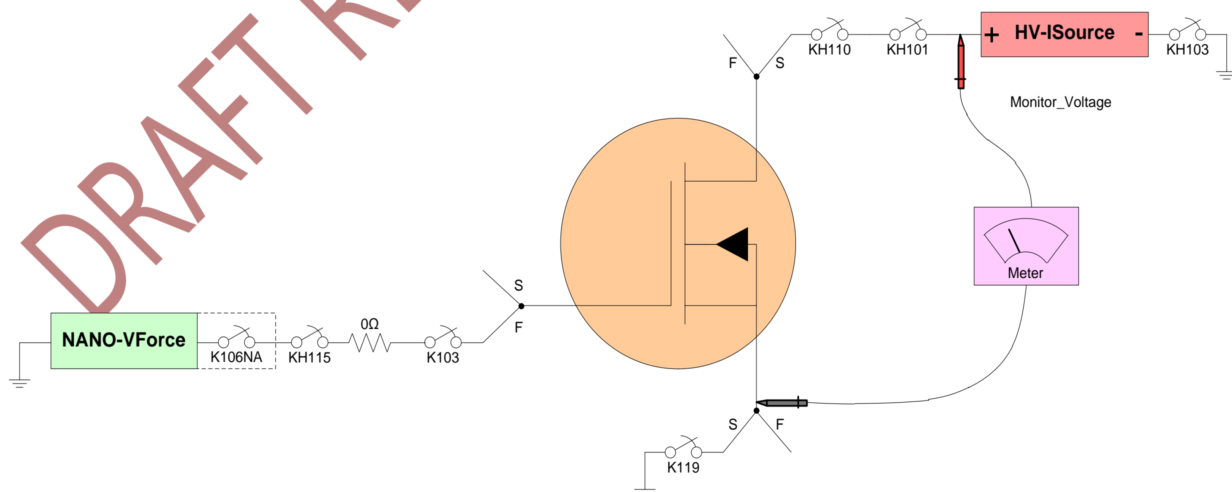
The Drain is connected to the HV current supply. Gate is connected to the Nano VForce supply that is set to a prior *VGS* test result times the *VX* parameter value. Note that the Nano VForce supply is limited to +/-25V.

The test runs by forcing a current of *ID* into the Drain pin, forcing a Gate, and measuring the breakdown voltage as measured from the HV current supply.

The *BVDSS_Max* limit is optional (use NaN or None if maximum limit is not desired), but there must be a minimum limit.

BVDSX Test Schematics

Configuration for N-Channel device.



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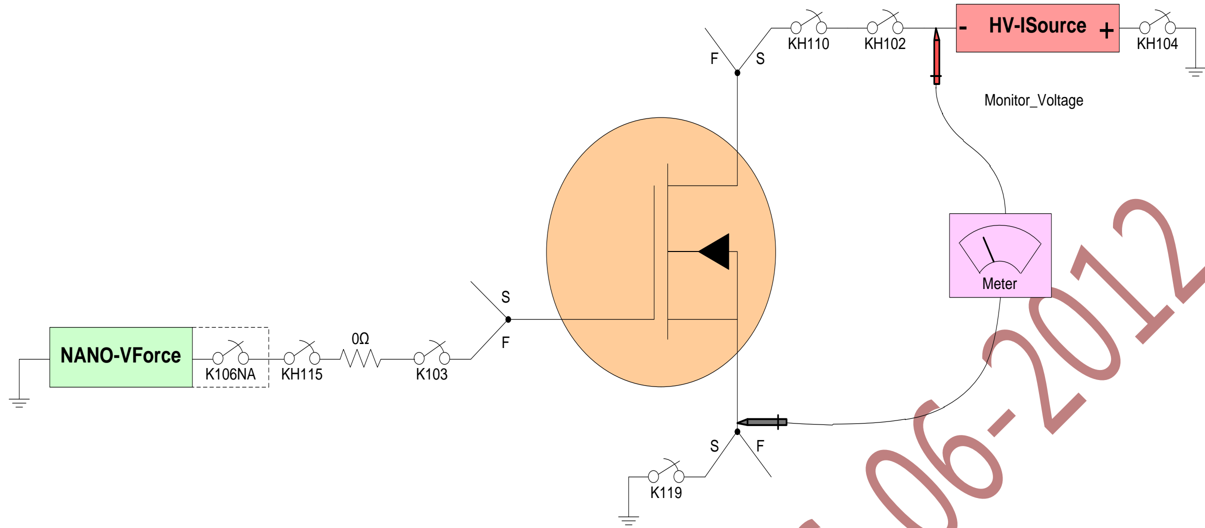
Configuration for P-Channel device.



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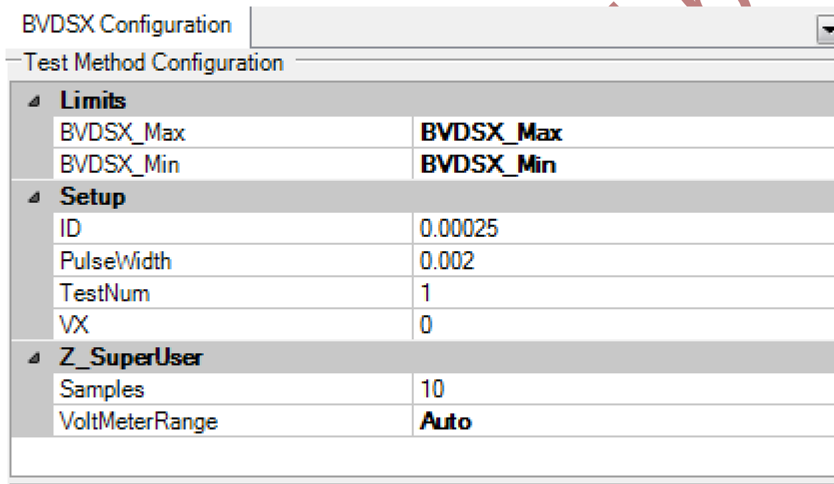
BVDSX Test Parameters



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BVDSS_Max ***BVDSS_Min***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. These values define the upper and lower limits of the break-down voltage result. *BVDSS_Max* may be NaN or None.
ID	Current to apply across the Drain-Source.
PulseWidth	Length of time, in seconds, to apply current.

	This must be set long enough for the power to rise fully. With longer cables, or coaxial cables going to a prober, extra time will need to be used, especially with higher voltage devices. So the pulse width must be increased until a stable reading is reached. Adjust the pulse (increase the pulse width) until a stable reading is achieved.
TestNum	Specifies the prior test and subtest number, in the form of **test.subtest**, in order to obtain the VGS voltage result that will be multiplied by the *VX* parameter and applied to the Gate during the break-down test.
VX	Defines a multiplication value to apply to the Gate voltage value obtained from a prior test. The prior test is defined by the *TestNum* parameter.
Samples	Number of measurement samples to average result. Sample rate is 11.6usec per sample. If the quantity of *Samples* is changed, *PulseWidth* may need to adjust accordingly.
VoltMeterRange	Provide means to force a voltage measurement range. Default automatically picks range based on *BVDSS_Max*. If *BVDSS_Max* is NaN or None, then range is determined by *BVDSS_Min* + 300. If the range is less than the break-down voltage, the reported voltage will be the maximum result provided by the range.

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BVGSO Test

Overview:

Measure the breakdown voltage across Gate to Source when significant current begins to flow between Gate and Source.

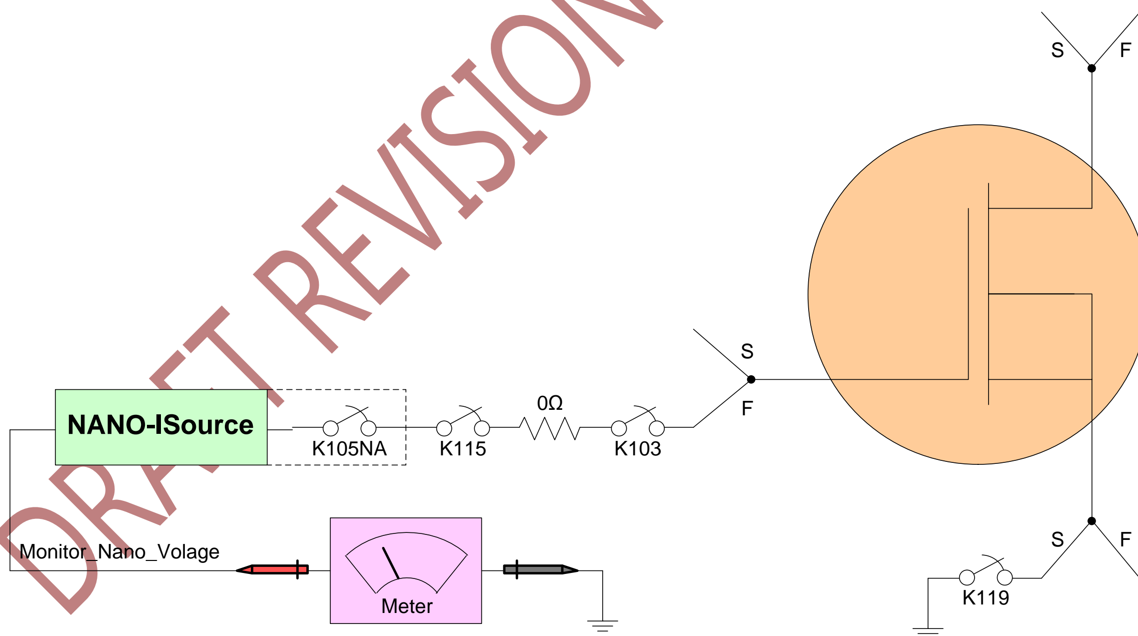
Description:

Apply a small current from Gate to Source and measure the voltage across the Gate-Source protection zener diode.

The test has the ability to measure both zener diode directions and log both results.

BVGSO Test Schematics

N-Channel or P-Channel configurations measuring BVGSO_POS and BVGSO_NEG conditions when all BVGSO_POS and BVGSO_NEG limit(s) are less than or equal to +/-25V.



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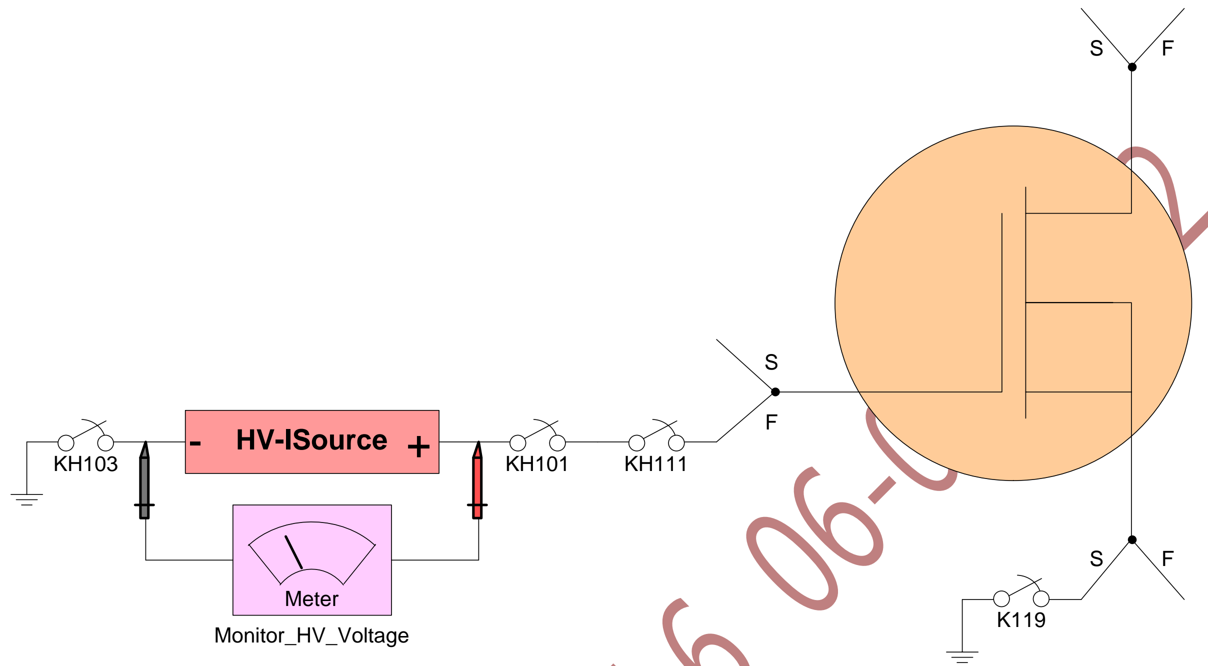
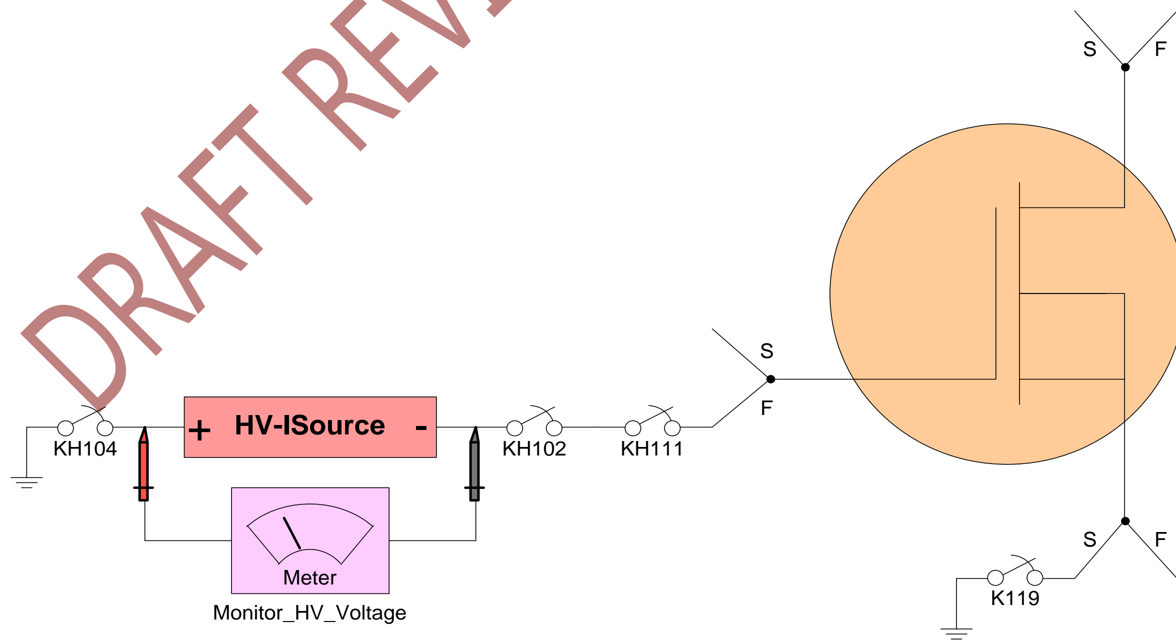
Configuration for N-Channel or P-Channel devices measuring BVGSO_POS when all limit(s) are greater than 25V.



Configuration for N-Channel or P-Channel devices measuring BVGSO_NEG when all limit(s) are greater than 25V.



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BVGSO Test Parameters

BVGSO Configuration

Test Method Configuration

Limits	
BVGSO_NEG_Max	**BVGSO_NEG_Max**
BVGSO_NEG_Min	**BVGSO_NEG_Min**
BVGSO_POS_Max	**BVGSO_POS_Max**
BVGSO_POS_Min	**BVGSO_POS_Min**
Misc	
PulseWidth	0.0007
Samples	10
Setup	
IG	0.00025

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BVGSO_NEG_Max ***BVGSO_NEG_Min***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. These values define the negative zener break-down voltage result limits..
BVGSO_POS_Max ***BVGSO_POS_Min***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. These values define the positive zener break-down voltage result limits.
PulseWidth:	Length of time, in seconds, to apply each voltage pulse. This is variable depending on the component(s) being tested. Adjust the pulse (increase the pulse width) until a stable reading is achieved.
Samples:	Number of measurement samples to average result. (Sample rate is 11.6usec per sample.) Ten (10) is normally adequate, but at lower currents, or with more noise, more samples may be required. If the number of samples is increased, *PulseWidth* may need to be increased to match. For example 100 samples would take 1.16msec, so with the default *PulseWidth* of 2msec, this only allows 0.84 msec for the voltage to stabilize, which would be enough for low

	voltages, but above 100V this would probably mean that the voltage had not settled, and so the first few samples would skew the accuracy of the reading. If you try to reduce *PulseWidth* so that it is less than the time required to make the measurements, the software will generate an alarm each time the test runs. Measurement samples are taken at the end of the pulse.
IG:	Gate current, in amps, to apply during pulses.

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ConnectionTest Test

Overview:

Test that the device is making good contact with socket, handler, or probe pins.

ConnectionTest test provides a fixed quantity of logged results and is limited to 25mA test current. Voltage is limited to +10V at DUT pins.

CONTINUITY test performs the same series summed resistance but will not break the resistance down into the three components of Gate, Drain, and Source. *CONTINUITY* uses a fixed 25mA forcing current. Voltage is limited to +36V at DUT pins.

KELVIN test quantity of logged results can vary, depending on the series summed resistance and other settings. *KELVIN* is limited to 100mA test current. Voltage is limited to +10V at the DUT pins.

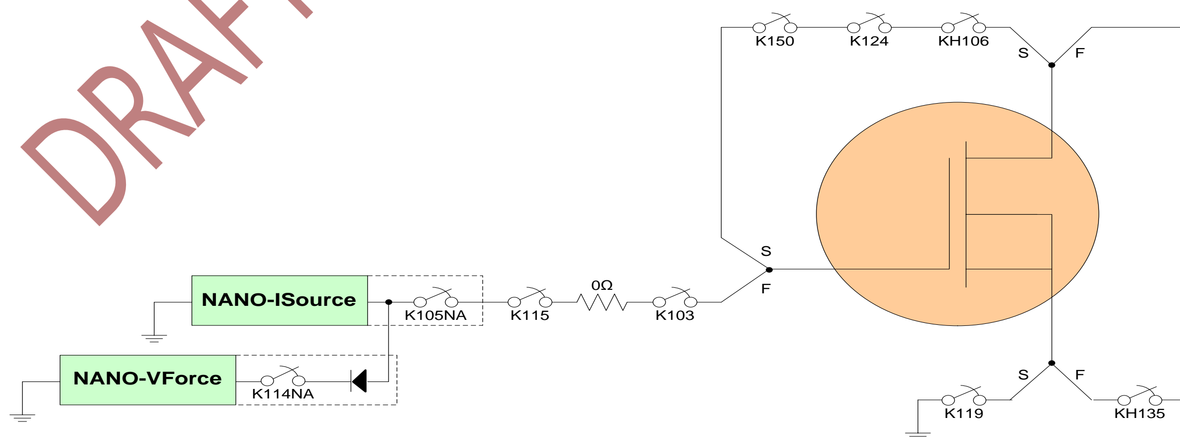
Description:

The continuity test is performed by placing *I_Apply* current through the Force and Sense socket (or contact) pins of Gate, Drain, and Source. If electron flow is inhibited by broken conductors, damaged components, or excessive resistance, the circuit is "open".

ConnectionTest will log the entire path resistance, and if enabled, the three components of Gate, Drain, and Source contact resistances.

Connection Test Schematic

Configuration for N-Channel or P-Channel devices.



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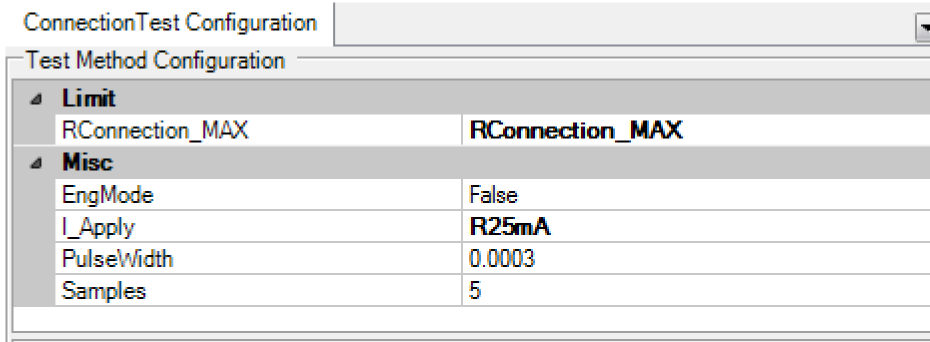
Connection Test Parameters



RConnection_MAX	This parameter is defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. Defines maximum allowed series summed resistance.
EngMode	True to measure and additionally log the three components of the series summed resistance values; Drain, Source, and Gate.
I_Apply	Amount of current to apply. Must be 25mA or less.
PulseWidth	Amount of time, in seconds, to apply current.
Samples	Number of measurement samples to average for each measurement. Sample rate is 11.6usec per sample. If *Samples* is increased, may need to increase *PulseWidth* accordingly.

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Continuity Test

Overview:

Test that the device is making good contact with socket, handler, or probe pins.

ConnectionTest test provides a fixed quantity of logged results and is limited to 25mA test current. Voltage limited to +10V at DUT pins.

CONTINUITY test performs the same series summed resistance but will not break the resistance down into the three components of Gate, Drain, and Source. *CONTINUITY* uses a fixed 25mA forcing current. Voltage is limited to +36V at DUT pins.

KELVIN test quantity of logged results can vary, depending on the series summed resistance and other settings. *KELVIN* is limited to 100mA test current. Voltage is limited to +10V at the DUT pins.

Description:

The continuity test is performed by placing a small current of 25mA across the Force and Sense socket (or contact) pins. If electron flow is inhibited by broken conductors, damaged components, or excessive resistance, the circuit is "open". The continuity test takes a Kelvin connection, force and sense of all 3 nodes and runs in series to provide an output of the total path resistance.

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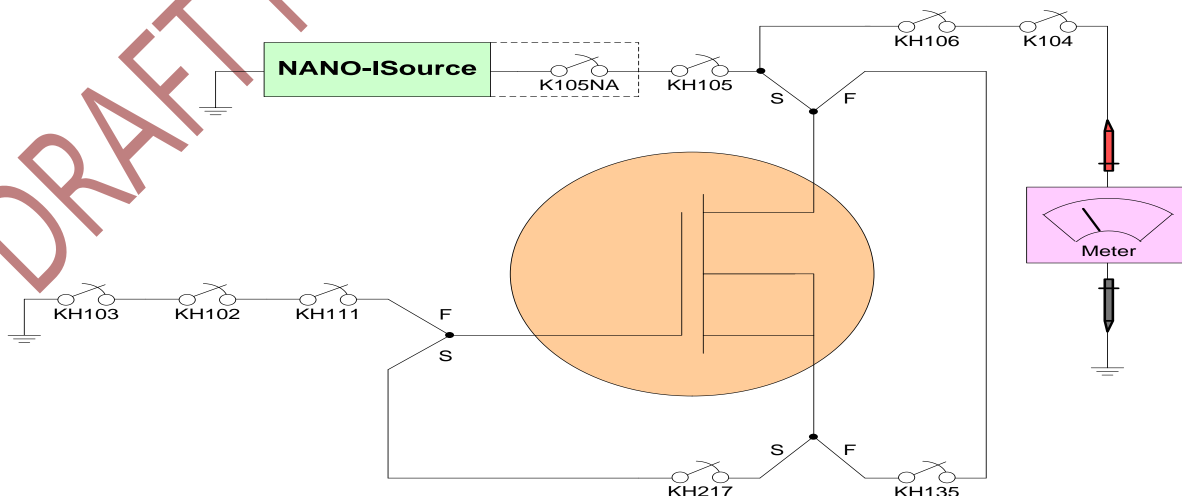
Continuity Test Schematic

Configuration for N-Channel or P-Channel devices.



Continuity Test Parameters

Continuity Configuration

Test Method Configuration

Limits	
Cont_Max	**Cont_Max**

Cont_Max	This parameter is defined on the *Program Variables* tab or can be changed by directly typing a value in the field.

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DrainToDrainOpenShort Test

Overview:

Breakdown voltage or, BVDSS, is the voltage at which the reverse-biased body-drift diode breaks down and significant current starts to flow between the Source and Drain. Typically the Gate to Source voltage will be 0 volts.

Description:

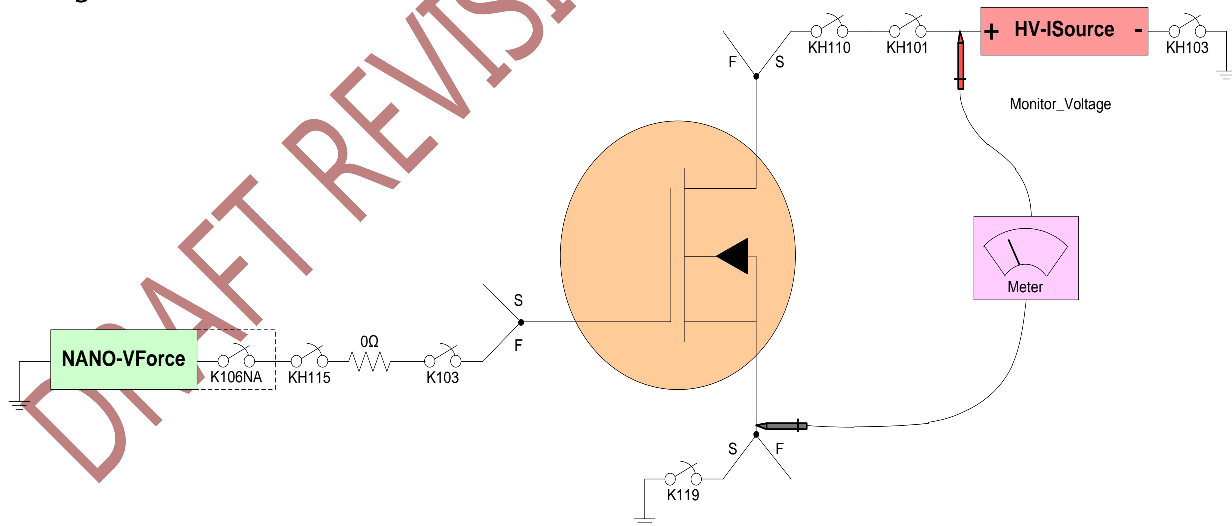
The Drain is connected to either 800V or 1200 HV Source depending on the version of HV supply the system has. Gate is connected to the NaVForce that can provide a gate voltage of up to +/- 25V.

The test runs by forcing a current (*ID*, typically 250uA) into the drain pin, forcing a Gate voltage (*VGS*), and measuring the breakdown voltage.

The max limit is optional. Use NaN or None if maximum limit is not desired. However, there must be a minimum limit.

DrainToDrainOpenShort Test Schematics

Configuration for N-Channel device.



Configuration for P-Channel device.

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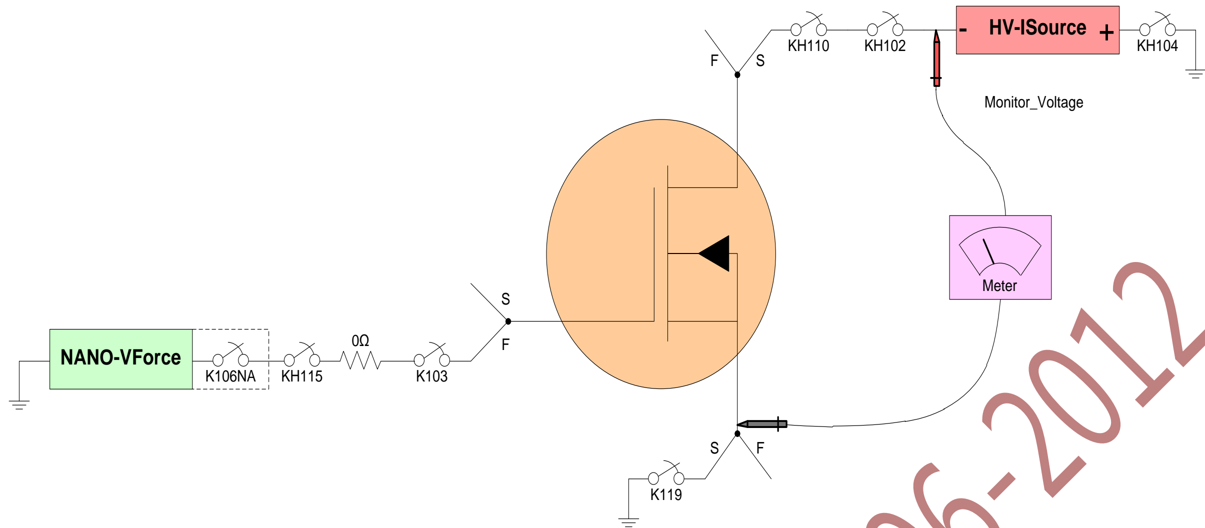

DrainToDrainOpenShort Test Parameters

DraintoDrainOpenShort Configuration

Test Method Configuration

Mics	
PulseWidth	0.001
Samples	10
Setup	
ClampVoltage	10
ID	0.001

Pulse width	Length of time, in seconds, to apply voltage. This must be set long enough for the power to rise fully. With longer cables, or coaxial cables going to a prober, extra time will need to be used, especially with higher voltage devices. So the pulse width must be increased until a stable reading is reached.
Samples	Number of measurement samples to average result. Sample rate is 11.6usec per sample. Ten (10) is normally adequate, but at lower currents, or with more noise, more samples may be required. If the number of samples is increased, *PulseWidth* may need to be increased to match. For example 100 samples would take 1.16msec,

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	so with the default *PulseWidth* of 2msec, this only allows 0.84 msec for the voltage to stabilize, which would be enough for low voltages, but above 100V this would probably mean that the voltage had not settled, and so the first few samples would skew the accuracy of the reading. If you try to reduce *PulseWidth* so that it is less than the time required to make the measurements, the software will generate an alarm each time the test runs. Measurement samples are taken at the end of the pulse.
ClampVoltage	Maximum VDS allowed during current pulse.
ID	Current to apply across Drain-Source.

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DVSD Test

Overview:

This test is used to ensure that the die is well attached to the lead frame in the package. It is sometimes also called a transient thermal resistance test, as it measures the thermal resistance from Junction to Ambient for a short pulse.

The *DVSD* test is limited to +/-30V VDS, 10A ID, and 150W.

Description:

The test closes SW2 and SW4, opens SW1 and SW3, and forces a small *IF_meas* current (typically 10mA) applied from Source to Drain and measures the FET intrinsic diode voltage drop.

Next, SW2 and SW4 are opened and SW1 and SW3 are closed. Voltage is applied to the Gate, and *VDS_heat* voltage applied from Drain to Source. The device is placed in a servo loop for the time duration of *TIME_heat* where the Gate voltage is adjusted to maintain the specified *ID_Heat* current.

Finally, the Gate is shut off, SW1 and SW3 opened and SW2 and SW4 are closed. The *IF_meas* current is again applied from Source to Drain to measure the diode drop after heating.

The difference in Vsd voltage is proportional to the temperature rise of the die. If the die is badly attached, then the thermal resistance will be high, and so the temperature rise will be higher. A well attached die will show lower temperature rise.

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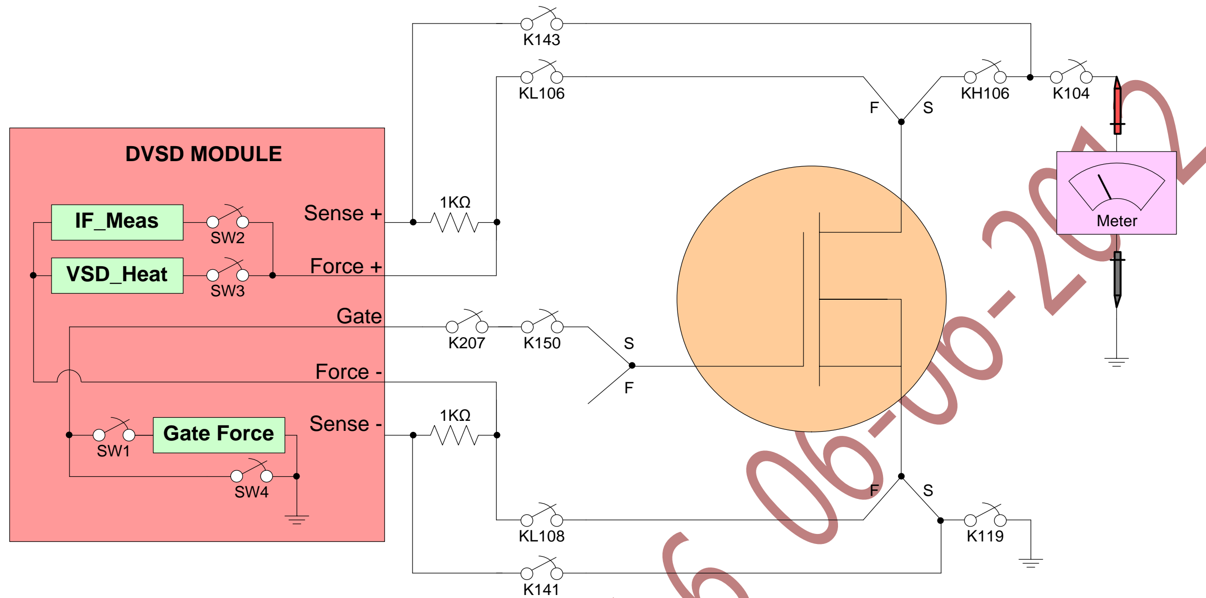
DVSD Test Schematic

Configuration for N-Channel or P-Channel devices. Device polarity is switched inside the DVSD Module.



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DVSD Test Parameters

DVSD Configuration	
Test Method Configuration	
Limits	
dVSD_Max	**dVSD_Max**
dVSD_Min	**dVSD_Min**
dVSD_VSD_Max	**dVSD_VSD_Max**
Misc	
CoolOffTime	0
CurrCompSlow	False
Dly_Before_Meas	3E-05
GateResistor	**R_1K**
Kfactor	2
Samples	40
VsdData	True
ZthData	False
Setup	
ID_Heat	1
IF_meas	0.01
TIME_heat	0.02
VDS_heat	8

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dVSD_MAX ***dVSD_MIN***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. These provide the upper and lower limits of the deltaVsd heating result.
dVSD_VSD_Max	This parameter is defined on the *Program Variables* tab or can be changed by directly typing the value in the field. This parameter provides a Vsd value that is used by the measurement instrument to define the measurement range. A value of 1, or less, is ideal as this will provide the best measurement resolution for most diodes.
CoolOffTime	Length of time, in seconds, to delay the test flow after the final Vsd measurement is preformed. This can be used to allow the die to cool before proceeding with the next test in the test flow.
CurrCompSlow	True to slow down the VDS/ID supply response time. False is normal instrument behavior.

Dly_Before_Meas	Amount of time, in seconds, to delay the final Vsd measurement following the heating pulse.
GateResistor	Provides the ability to change the Gate series resistance. Increasing the series Gate resistance often eliminates device oscillation during the heating pulse servo operation.
Kfactor	Value (mv/°C) used to compute the Thermal Impedance of the device. (*ZthData* flag must be True in order to log the Thermal Impedance value.) °C/W = (Abs(finalVsd – initialVsd) / (*Kfactor* / 1000)) / (*ID_Heat* * *VSD_heat*)
Samples	Number of measurement samples for Vsd measurements. Initial Vsd measurement will limit to 10 samples.
VsdData	True to log initial and final Vsd data values.
ZthData	True to log Thermal Impedance value. (Requires *Kfactor* value for computation.)
ID_Heat	Defines the amount of ID current (amps) to maintain during the heating pulse.
IF_Meas	Defines the amount of current (amps) to apply to the Intrinsic Diode for initial and final Vsd measurement.
TIME_Heat	Duration of heating pulse, in seconds.
VDS_heat	Defines the VDS voltage to apply during the heating pulse.

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DVSD_using_HPM Test

Overview:

This test is used to ensure that the die is well attached to the lead frame in the package. It is sometimes also called a transient thermal resistance test, as it measures the thermal resistance from Junction to Ambient for a short pulse.

The *DVSD_using_HPM* test is limited to 55V, 100A, or 12W.

Description:

The test starts by disabling the heating current source on the HP module and enable the *IF_meas* current to flow through the FET intrinsic diode. The voltage across the diode (Vsd) is measured.

Next, *ID_Heat* is applied and the Gate voltage is adjusted to maintain a constant voltage across the Drain-Source for the *TIME_heat* time.

The Gate is quickly taken to GND (effectively tied to Drain) and *ID_Heat* current is removed. With the *IF_meas* current flowing through the intrinsic diode, the diode voltage (Vsd) is again measured.

The difference between the Vsd prior to the heating pulse and the Vsd after the heating pulse is logged.

The amount of temperature rise (Zth) can be logged if the *ZthData* flag is true and a proper *Kfactor* is provided.

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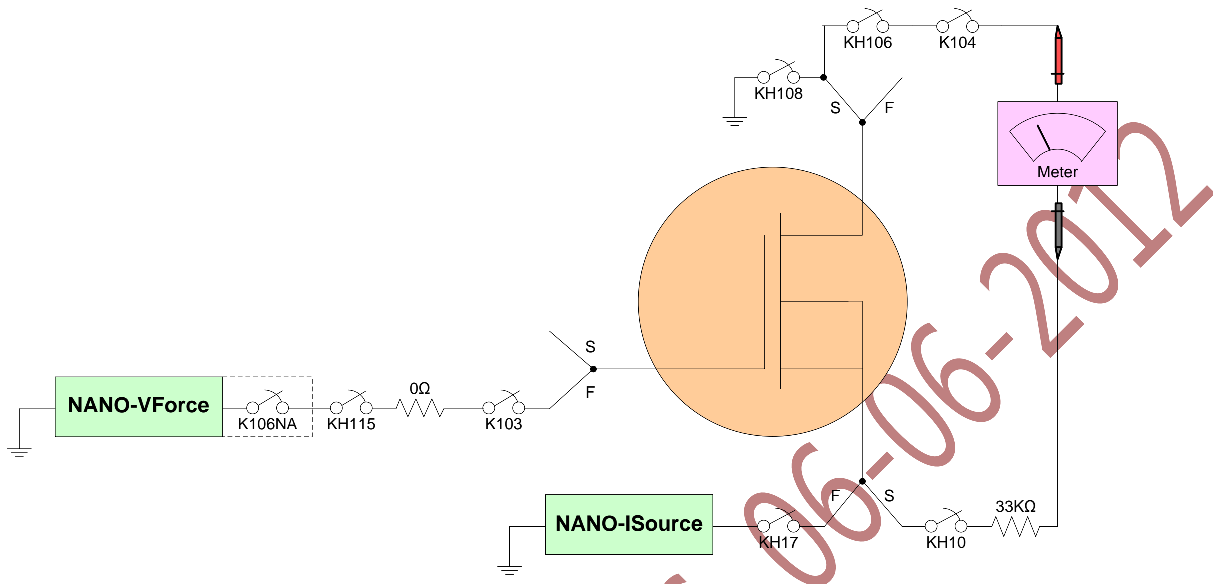
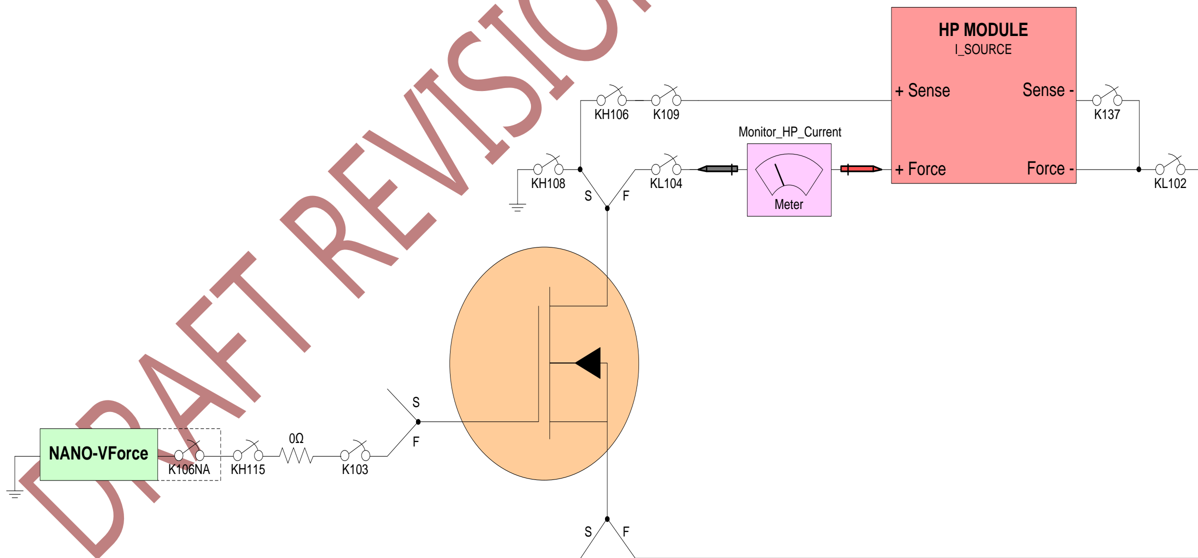
DVSD_using_HPM Test Schematic

Configuration for N-Channel or P-Channel devices when measuring VSD.



Configuration for N-Channel for heating pulse phase.



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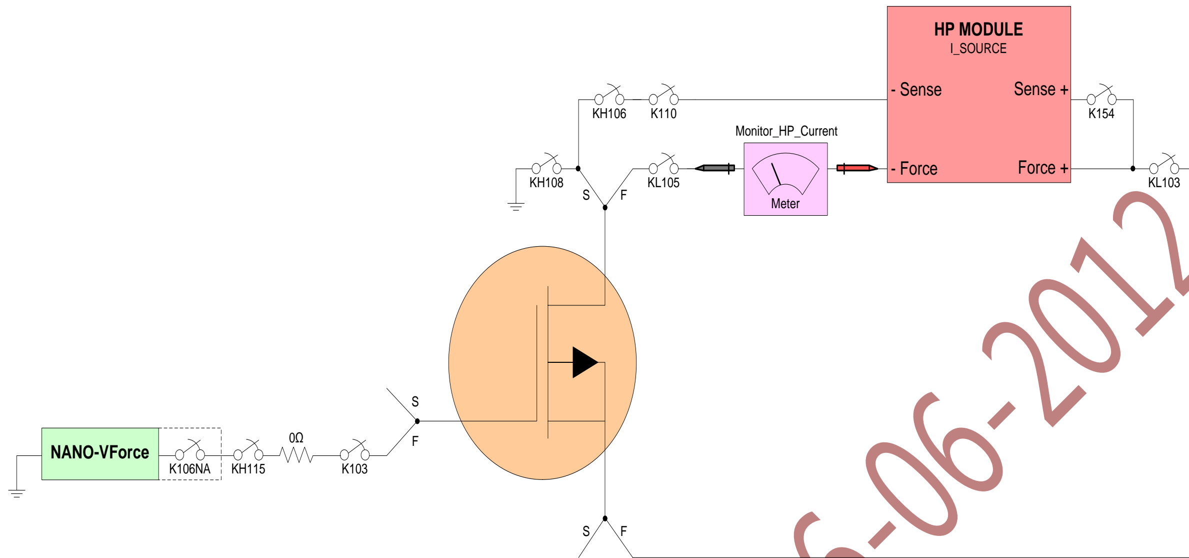
Configuration for P-Channel for heating pulse phase.



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DVSD_using_HPM Test Parameters

DVSD_using_HPM Configuration

Test Method Configuration

Parameter	Value
Limits	
dVSD_Max	**dVSD_Max**
dVSD_Min	**dVSD_Min**
Misc	
DebugMode	False
Dly_Before_Meas	3E-05
Kfactor	2
Samples	4
Vgate	0
VsdData	**False**
ZthData	**False**
Setup	
ID_Heat	1
IF_meas	0.01
TIME_heat	0.02
VDS_heat	8

dVSD_MAX ***dVSD_MIN***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields.

	These provide the upper and lower limits of the deltaVsd heating result.
DebugMode	True to log additional test data, such as starting and stored (for next DUT test) Gate voltages. True will also override automatic initial Gate voltage mode. (Refer to *Vgate* description for more information.)
Dly_Before_Meas	Amount of time, in seconds, to delay the final Vsd measurement following the heating pulse.
Kfactor	Value (mv/°C) used to compute the Thermal Impedance of the device. (*ZthData* flag must be True in order to log the Thermal Impedance value.) °C/W = (Abs(finalVsd – initialVsd) / (*Kfactor* / 1000)) / (*ID_Heat* * *VSD_heat*)
Samples	Number of measurement samples to average for initial Vsd measurement. Final Vsd measurement, after heating pulse, is fixed to three (3) samples. Sample rate is 11.6usec per sample.
Vgate	Means to override initial Gate voltage applied at the beginning of the heating pulse. If the initial Gate voltage is greatly different than the achieved regulating heating pulse Gate voltage, the amount of total power applied to the DUT will be either greater or less than the desired power. The test will store the achieved regulating Gate voltage for the next device. It is assumed that the Gate voltage will be similar within the same device family parts. NOTE: In order to override automatic initial Gate voltage value, *DebugMode* must also be True.
VsdData	True to additionally log initial and final Vsd data values.

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ZthData	True to additionally log Thermal Impedance value. (Requires *Kfactor* value for proper computation.)
ID_Heat	Defines the amount of ID current, in amps, to maintain during the heating pulse.
IF_meas	Defines the amount of current, in amps, to apply to the Intrinsic Diode for initial and final Vsd measurement.
TIME_Heat	Duration of heating pulse, in seconds.
VDS_heat	Defines the VDS voltage to apply during the heating pulse.

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Gate_Stress Test

Overview:

Generate a variable length IGSS pulse and monitor Gate leakage. If leakage is too high, terminate pulse.

> *IGSS* test may not function properly for long pulses, and does not terminate the pulse if the leakage gets too high.

Description:

With K116 closed, measure offset voltage. Open K116, apply Gate voltage (by applying voltage to Drain and Source in opposite polarity of VGS), delay some amount of time for Cg effects in association with the current measurement sense resistor, and then measure voltage across the current sense resistor.

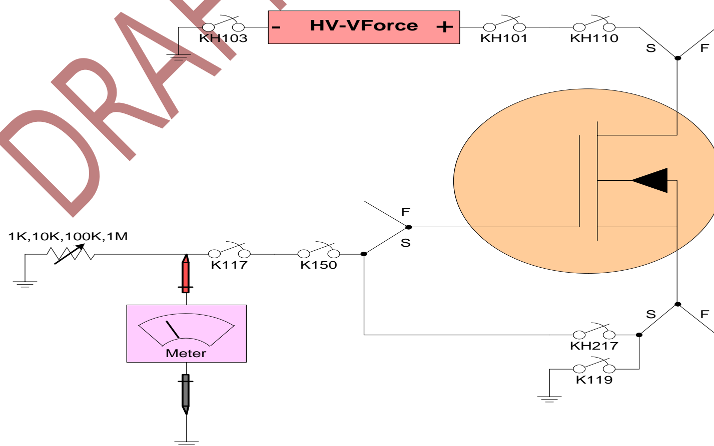
In order to improve result accuracy, a number of samples are averaged over 18ms of time. The *PulseWidth* must be long enough to include the 18ms measurement time, plus settle time due to the current range selection.

The settle time for current range selection is different for each range. 1uA range requires 25ms settle time. 10uA range requires 8ms, 100uA range requires 3ms, and 1mA range requires 2ms. The 10mA and 100mA ranges require 500usec of settle time. Settle time mostly accounts for DUT Cg effects in association with the series current range resistor value.

The leakage measurement may be disabled for decreased pulse times.

Gate_Stress Test Schematics

Configuration for positive *VGS* values.



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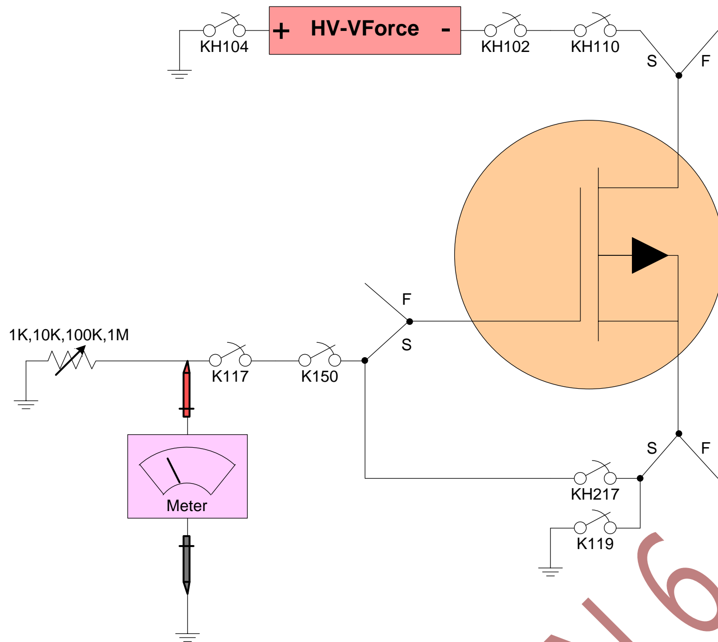
Configuration for negative *VGS* values.



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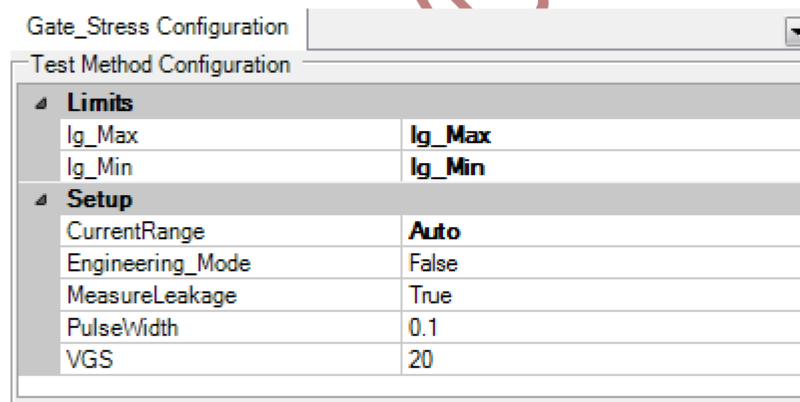
Gate_Stress Test Parameters



Gate_Stress Configuration

Test Method Configuration

Limits	
Ig_Max	**Ig_Max**
Ig_Min	**Ig_Min**
Setup	
CurrentRange	**Auto**
Engineering_Mode	False
MeasureLeakage	True
PulseWidth	0.1
VGS	20

Ig_Max ***Ig_Min***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. These values define the upper and lower limits of the Gate leakage result.

CurrentRange	Method to force current measurement range. If *CurrentRange* is Auto, range is computed from largest of |Ig_Max| or |Ig_Min|.
Engineering_Mode	Display and log additional measurement information.
MeasureLeakage	Enable (True) or disable (False) the current leakage measurement. When set to False and selecting the highest current range will reduce the pulse width to minimum.
PulseWidth	Length of time, in seconds, to apply voltage. This must be set long enough for the power to rise fully. With longer cables, or coaxial cables going to a prober, extra time will need to be used, especially with higher voltage devices. Adjust *PulseWidth*, typically increase, until a stable reading is achieved. The *PulseWidth* must be long enough to encompass measurement and instrument settle time. Settle time is dependent on the current measurement range. If a shorter *PulseWidth* is desired, it may be necessary to force a higher current range, at the sacrifice of measurement accuracy.
VGS	Amount of Gate voltage to apply during the test pulse. **NOTE**: The applied voltage will be independent of the global *DeviceType* selection. If a different Gate polarity is desired depending on N-Channel versus P-Channel device, the *VGS* parameter must be explicitly modified accordingly. The reason for this is because it may be desired to stress both a positive and negative Gate voltage on a single device.

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GFS

Overview:

Gate Forward & Gate Forward Digital. This test measures the gain of the FET. Limits are the minimum and maximum in gain in Siemens.

For the more traditional GFS test methodology, it is suggested using the *GMP* test instead.

The *GFS* test can perform the test with a smaller pulse width than the industry standard measurement method. The measurement result compensates for die heating effects.

Description:

VDS is applied to the Drain-Source. *VgsStart* is applied to the Gate. The Gate voltage is increased by *VgsStep* volts until at least _ID * 1.1_ amps is achieved or *VgsMax* is reached.

If _ID * 1.1_ amps is achieved, the Gate voltage is decremented by *VgsStep* volts until the current is less than _ID * 0.9_ amps, or *VgsStart* is reached.

Gain is computed as an average of the delta rising ID / delta rising Vgs and the delta falling ID / delta falling Vgs. Rising being defined as Vgs incrementing by *VgsStep* and falling being defined as Vgs decrementing by *VgsStep*.

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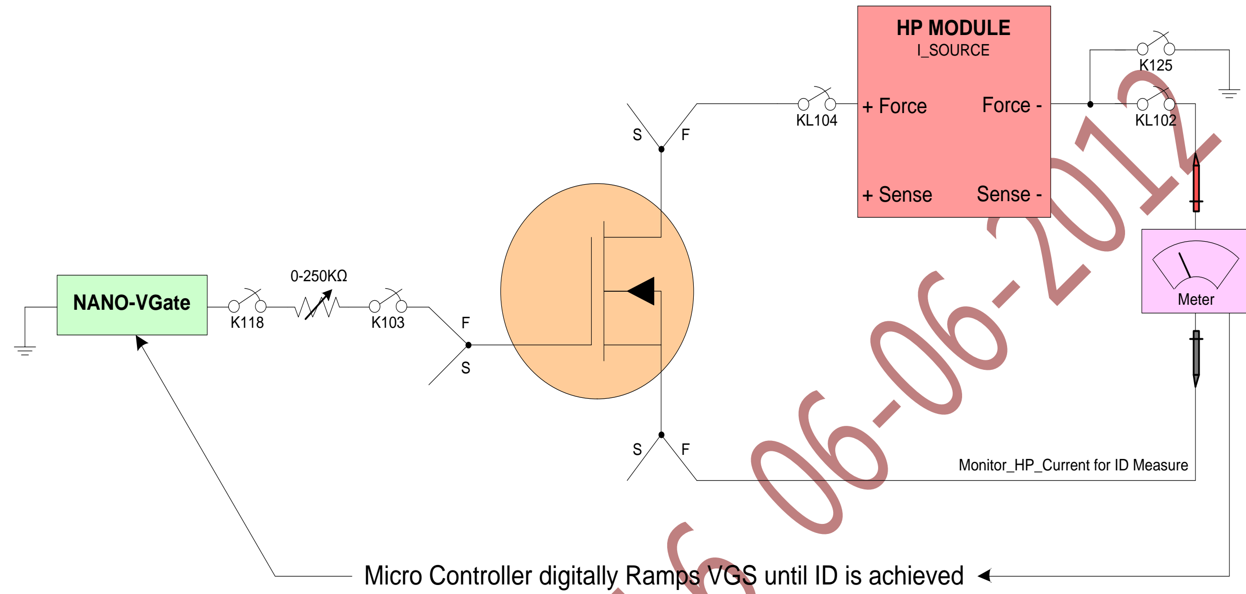
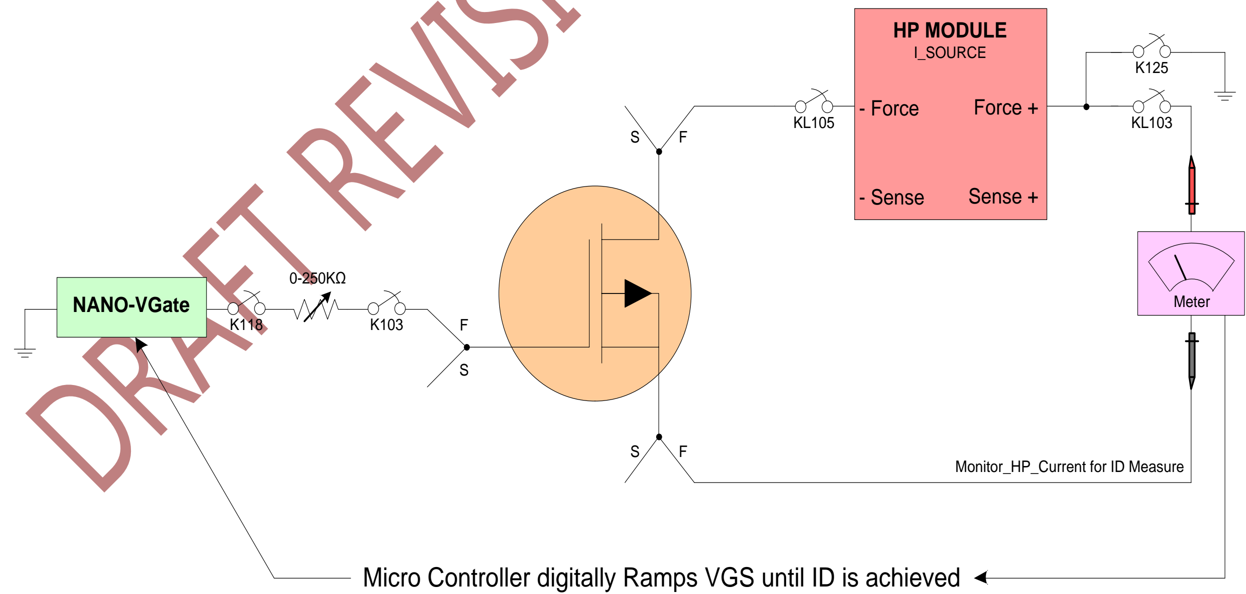
GFS Test Schematics

Configuration for N-Channel device.



Configuration for P-Channel device.



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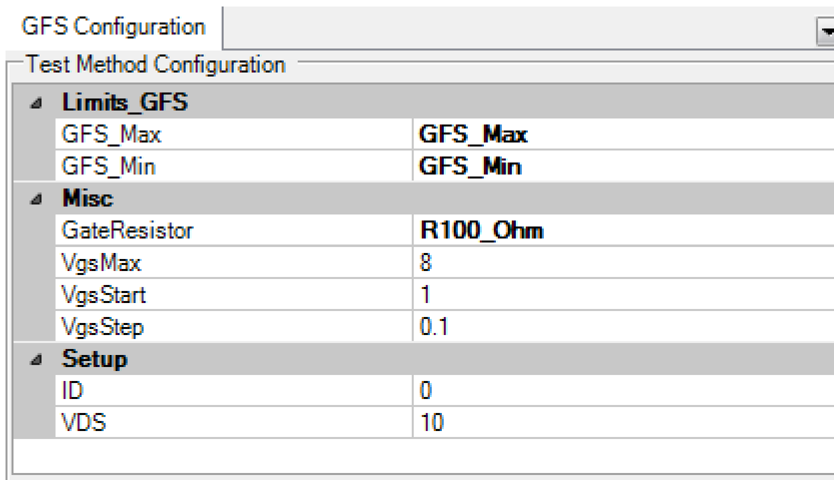
GFS Test Parameters



GFS_Max ***GFS_Min***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. These values define the upper and lower gain limits.
Gate Resistor	Based on component being tested, choose until oscillation stops.
VgsMax	Maximum voltage to apply to Gate.
VgsStart	Starting Gate voltage.
VgsStep	Gate increment step voltage (positive value), or decrement if negative value.
ID	Drain to Source current, in amps.
VDS	Drain to Source voltage to apply.

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GFS_digi Test

Overview:

This test measures the gain of the FET. Limits are the minimum and maximum in gain in Siemens.

The *GFS_digi* test can perform the test with a smaller pulse width than the industry standard measurement method. The measurement result compensates for die heating effects.

This test includes the ability to log additional data such as IDON, VGS, and VTH. The additional data is available from the single pulse used for GFS. This provides faster test time and less die heat generated.

Description:

VDS is applied to the Drain-Source. *VgsStart* is applied to the Gate. The Gate voltage is increased by *VgsStep* volts until at least the larger of *ID1* or *ID2* amps is achieved or *VgsMax* is reached.

If current is achieved, the Gate voltage is decremented by *VgsStep* volts until the current is less than the lesser of *ID1* or *ID2* amps, or *VgsStart* is reached.

Gain is computed as an average of the delta rising ID / delta rising Vgs and the delta falling ID / delta falling Vgs. Rising being defined as Vgs incrementing by *VgsStep* and falling being defined as Vgs decrementing by *VgsStep*.

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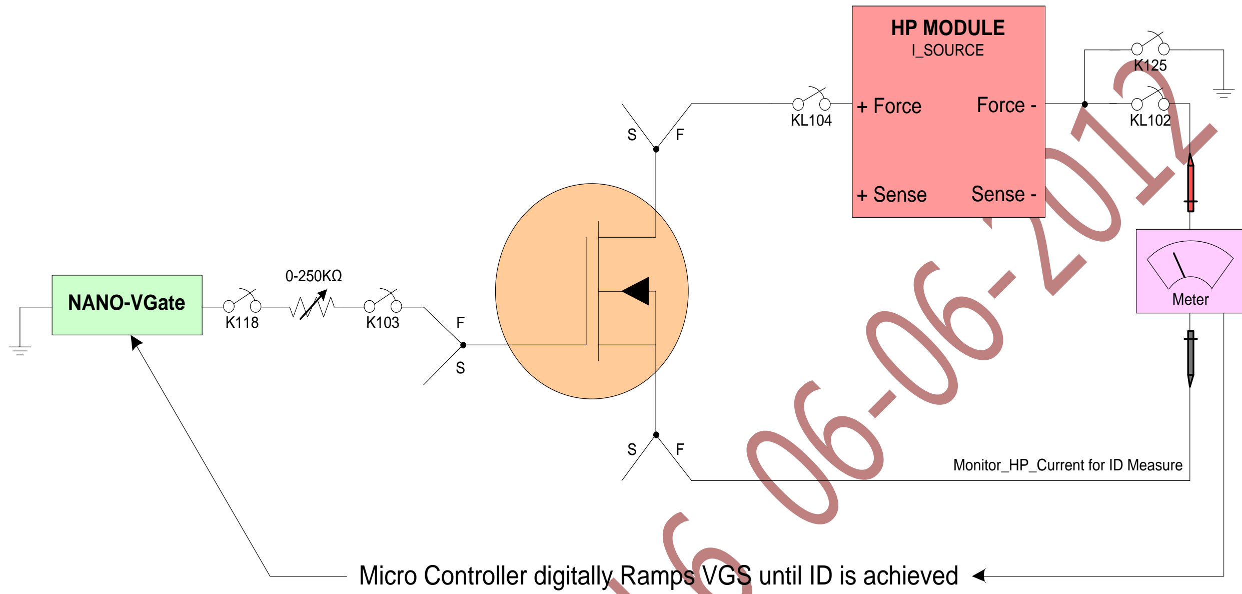
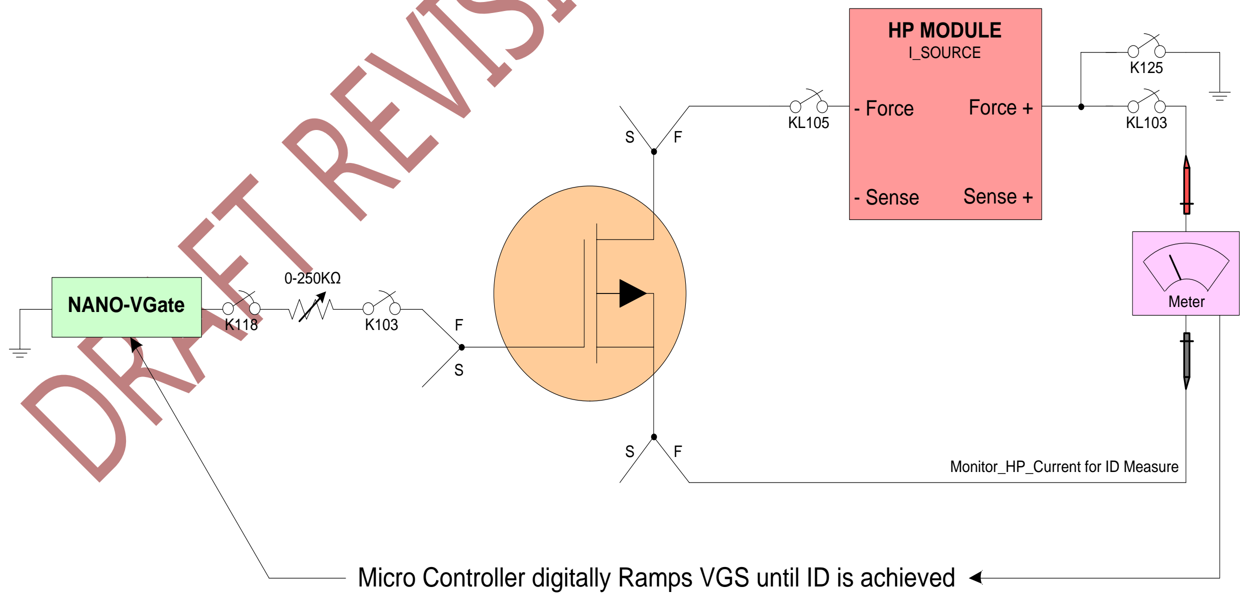
GFS_Digi Test Schematics

Configuration for N-Channel device.



Configuration for P-Channel device.



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GFS_digi Test Parameters

GFS_Digi Configuration

Test Method Configuration

Parameter	Value
Limits_GFS	
GFS_Max	**GFS_Max**
GFS_Min	**GFS_Min**
Limits_IDON	
IDON_Max	**IDON_Max**
IDON_Min	**IDON_Min**
Limits_VGS	
Delta_VGS_Max	**Delta_VGS_Max**
Delta_VGS_Min	**Delta_VGS_Min**
VGS1_Max	**VGS1_Max**
VGS1_Min	**VGS1_Min**
VGS2_Max	**VGS2_Max**
VGS2_Min	**VGS2_Min**
Limits_VTH	
VTH1_Max	**VTH1_Max**
VTH1_Min	**VTH1_Min**
VTH2_Max	**VTH2_Max**
VTH2_Min	**VTH2_Min**
Misc	
DebugData	**Off**
GateResistor	100
VgsMax	8
VgsStart	1
VgsStep	0.1
Misc_Enables	
Delta_Vgs_Enable	False
IDON_Enable	False
VGS_Enable	False
VTH_Enable	False
Setup	
ID1	0
ID2	5
VDS	10

Parameter	Description
GFS_Max ***GFS_Min***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. These values define the upper and lower gain limits.
IDON_Max ***IDON_Min***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields.

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	These values define the upper and lower IDON limits. The *IDON_Enable* flag must be True in order for these limits to be utilized.
Delta_VGS_Max ***Delta_VGS_Min***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. These values define the upper and lower dVGS limits. The *VGS_Enable* and *Delta_Vgs_Enable* flags must be True and both *ID1* and *ID2* must be defined in order for these limits to be utilized. The dVGS result is the difference in Vgs values that was required to achieve *ID1* and *ID2* currents.
VGS1_Max ***VGS1_Min***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. These values define the upper and lower Vgs result limits for *ID1* condition. The *VGS_Enable* flag must be True in order for these limits to be utilized, and *ID1* must be defined for valid result. VGS1 result is the Vgs voltage required to achieve *ID1* current.
VGS2_Max ***VGS2_Min***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. These values define the upper and lower Vgs result limits for *ID2* condition. The *VGS_Enable* flag must be True in order for these limits to be utilized, and *ID2* must be defined for valid result.

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	VGS2 result is the Vgs voltage required to achieve *ID2* current.
VTH1_Max ***VTH1_Min***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. These values define the upper and lower VTH result limits for *ID1* condition. The *VTH_Enable* flag must be True in order for these limits to be utilized, and *ID1* must be defined for valid result.
VTH2_Max ***VTH2_Min***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. These values define the upper and lower VTH result limits for *ID2* condition. The *VTH_Enable* flag must be True in order for these limits to be utilized, and *ID2* must be defined for valid result.
DebugData	True to enable logging of up to 200 Vgs and ID ramp data points.
Gate Resistor	Based on component being tested – choose until oscillation stops.
VgsMax	Maximum voltage to apply to Gate.
VgsStart	Starting Gate voltage.
VgsStep	Gate increment step voltage (positive value), or decrement if negative value.
Delta_VGS_Enable	True to enable logging of dVGS data results. Must also set *VGS_Enable* flag toTrue.

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IDON_Enable	True to enable logging of IDON data results.
VGS_Enable	True to enable logging of VGS data results.
VTH_Enable	True to enable logging of VTH data results.
ID1	Drain to Source current, in amps. Typically smaller absolute value than *ID2*, but is not required to be smaller. If not logging IDON, VGS, or VTH, *ID1* can be 0. If *ID1* is 0, will ramp Vgs until minimum of *ID2* is achieved. Will then use Vgs and current sample points on either side of *ID2* in order to compute gain.
ID2	Drain to Source current, in amps.
VDS	Drain to Source voltage to apply.

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GMP Test

Overview:

Measure the change in required VGS to get a prescribed change in ID.

> This is the recommended gain test. This test more closely adheres to the industry standard test method.

Description:

The GMP Test requires the drain current to be set to fixed levels of *ID1* and *ID2*, and the Vgs measured. The drain-source voltage also needs to be controlled. This is done by setting the gate at GND, and using the floating High Power supply to supply the drain current. The DUT will self bias to set the *Vgs*, by allowing the source to go to a negative voltage (for an N-Channel device, positive for a P-Channel device). The drain voltage is set to a fixed level, which adds to the Vgs, and so determines the Vds. The Vds cannot be set directly, and will vary as the Vgs varies. To minimize this effect, the limits are used to calculate the expected Vgs shift, and this is also used to adjust the Vd. For this reason, the actual measured Vds is logged for this test as well as the measured Gm.

As the tester does not know what Vgs the device will settle at, you need to set a *VgsNom* for the tester to calculate the initial Vd = *VDS* - *VgsNom* to set on the Drain. The current is set to *ID1*, then *ID2*, then back to *ID1*. The Vgs is measured at each step, and the GMP is calculated as (*ID2* - *ID1*) / (Vgs2 – Vgs3), where Vgs3 is the last one measured at *ID1* condition.

The first *ID1* is a calibration pulse, where the Vgs is measured at *ID1*. This is used to calculate the Vd used in the other steps which follow.

The parameter *CoolDownTime* can be used to allow a time between each pulse to control thermal effects. If set to zero, the calibration pulse (at *ID1*), and the two measurement pulses at *ID2* and *ID1*, are done in a single sweep with no cooling time between the pulses.

The *GMP* test is very sensitive to thermal effects, and so the settings of *VDS*, *ID1*, and *ID2* as well as *PulseWidth* may have large effects on the result. If *VDS* and ID is high, the device can be tested in a thermal runaway condition resulting in infinite, or negative, Gm. Also, *VDS* depends on the actual device Vgs, the values of the limits are used to attempt to adjust Vd to get the correct *VDS*. This means that changing the limits will affect the *VDS*, which may affect the Gm test result.

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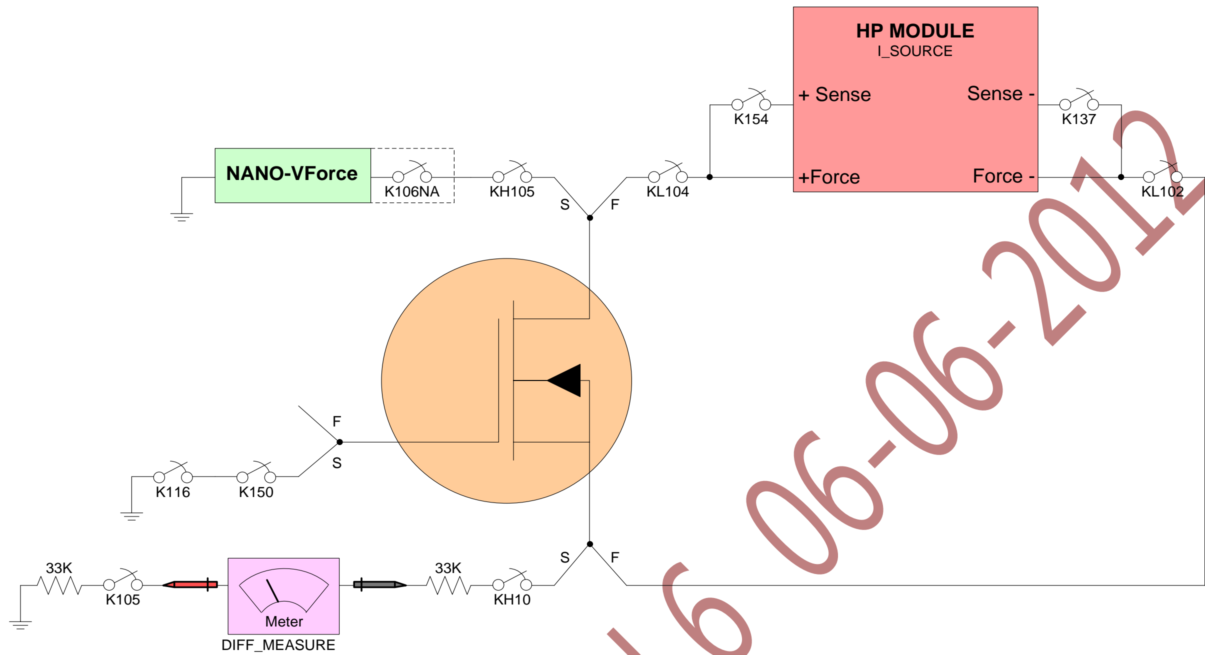
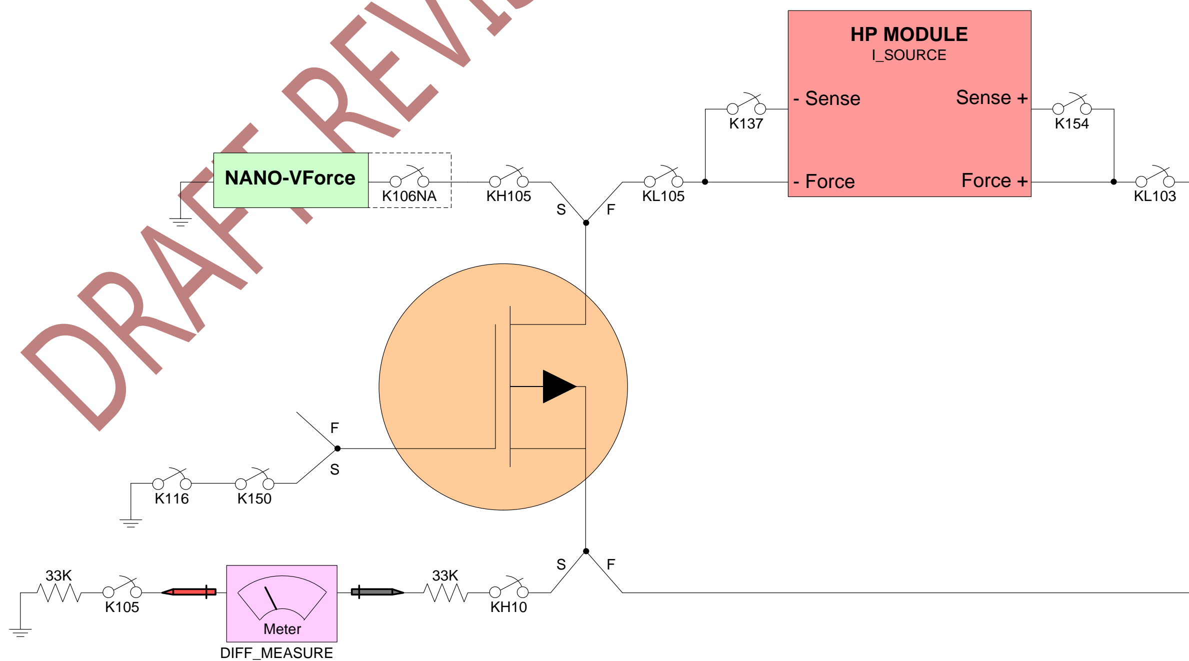
GMP Test Schematics

Condition for N-Channel device.



Condition for P-Channel device.



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GMP Test Parameters

GMP Configuration

Test Method Configuration

Limits_GMP	
GMP_Max	**GMP_Max**
GMP_Min	**GMP_Min**
Misc	
Gate Resistor	**R100_Ohm**
Samples	10
VgsNom	3
Setup	
CoolDownTime	0
ID1	1
ID2	10
Pulse Width	0.0005
VDS	10

GMP_Max ***GMP_Min***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. These values define the upper and lower gain limits.
Gate Resistor	Based on component being tested. Typically increase resistance until oscillation stops.
Samples	Define number of measurement samples for measurement averaging. (Sample rate is 11.6usec per sample.) If the quantity of samples is increased, it may become necessary to increase the *PulseWidth*.
VgsNom	Define a nominal starting Gate voltage. Actual Gate voltage will be determined during ID pulse.
CoolDownTime	Amount of time, in seconds, to allow device to cool between pulses.
ID1	Current, in amps, for first ID pulse.
ID2	Current, in amps, for second ID pulse.
PulseWidth	Width of pulses, in seconds.

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VDS	Drain-Source voltage to apply during pulse.

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IDON Test

Overview:

Test current capability of MOSFET at a specific Gate voltage.

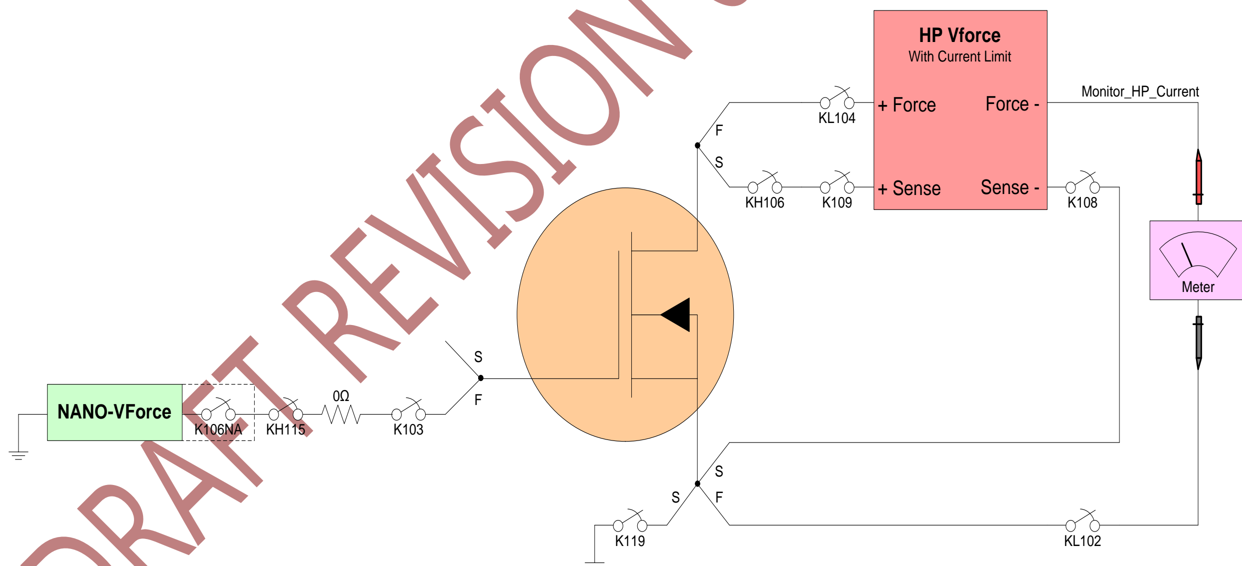
Description:

Apply *VGS* voltage to the Gate and *VDS* voltage to the Drain-Source and measure current that the FET is capable of conducting.

VDS supply current is limited to two (2) times the IDON_Min value, or if |IDON_Max| is greater than 0.1, the current is limited to IDON_Max * 1.1.

IDON Test Schematics

Configuration for N-Channel device.



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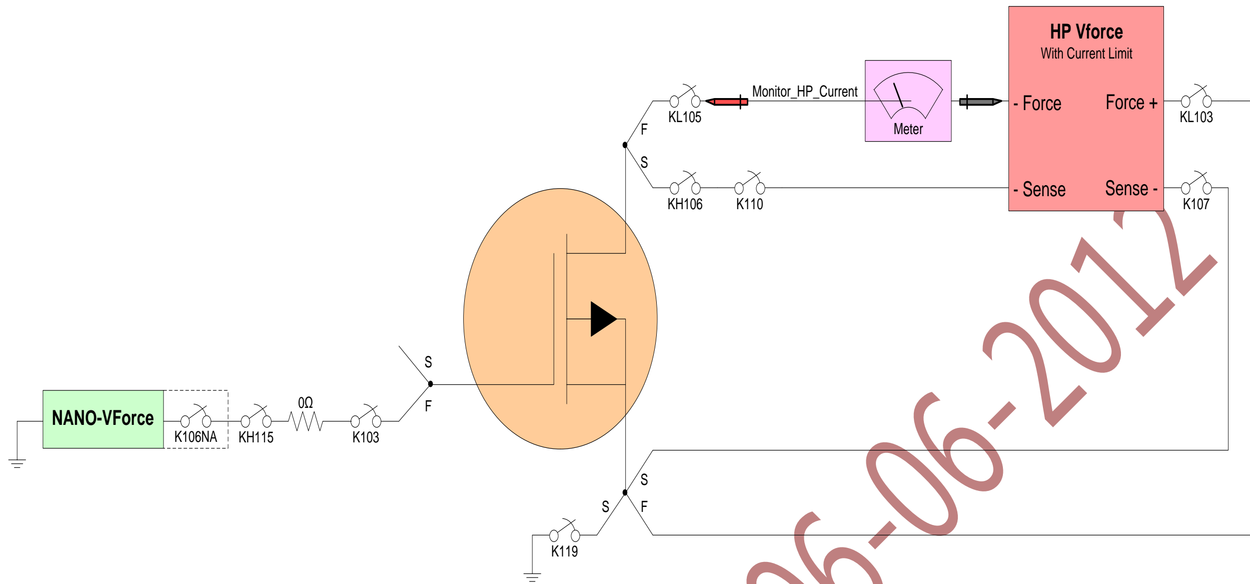
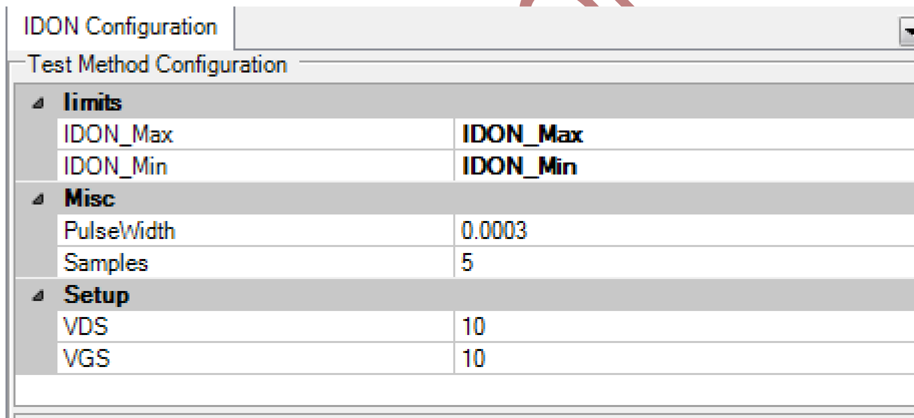
Configuration for P-Channel device.



IDON Test Parameters



IDON Configuration

Test Method Configuration

limits	
IDON_Max	**IDON_Max**
IDON_Min	**IDON_Min**
Misc	
PulseWidth	0.0003
Samples	5
Setup	
VDS	10
VGS	10

IDON_Max ***IDON_Min***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. These values are dependent upon device specification.
PulseWidth	Length of time in seconds to apply each voltage pulse. This is variable depending on the component(s) being tested. Adjust the pulse (ramp up the length) until a stable reading

	is achieved.
Samples	Number of pulses to be applied during the pulse width. Sample rate is 11.6usec per sample. If the quantity of samples is increased, it may be necessary to increase the *PulseWidth*.
VDS	Specified Drain-Source voltage.
VGS	Specified Gate-Source voltage to apply.

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IDSS Test

Overview:

Measure amount of Drain to Source current leakage of MOSFET.

Description:

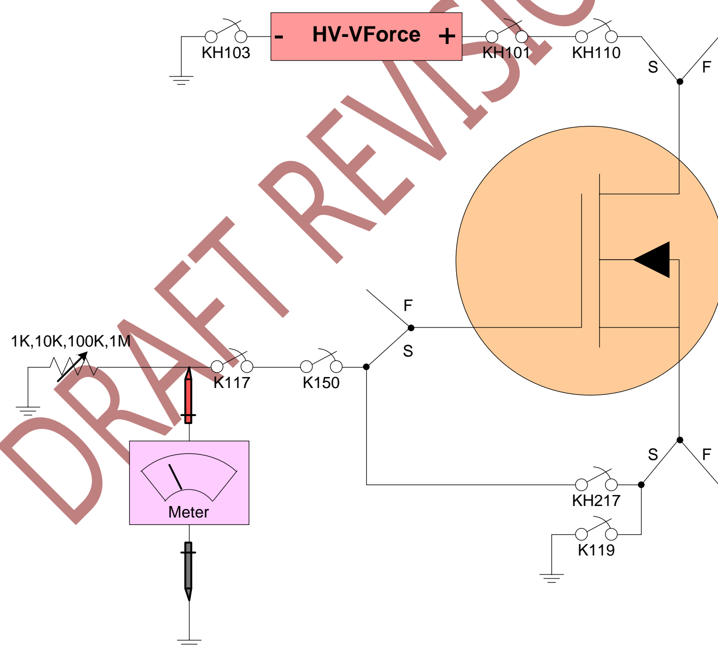
Supply instrument used and measurement accuracy is dependent on *VDS* voltage parameter value.

VDS voltages greater than +/-25V will use the HV supply module. The lowest current range of the HV supply module is 10ua, which is not accurate for leakage currents less than 100na.

The test will set the Gate to *VGS* volts and set the appropriate supply to *VDS* volts and measure the leakage current at the end of the pulse defined by *PulseWidth*.

IDSS Test Schematics

Configuration for N-Channel device using HV supply.



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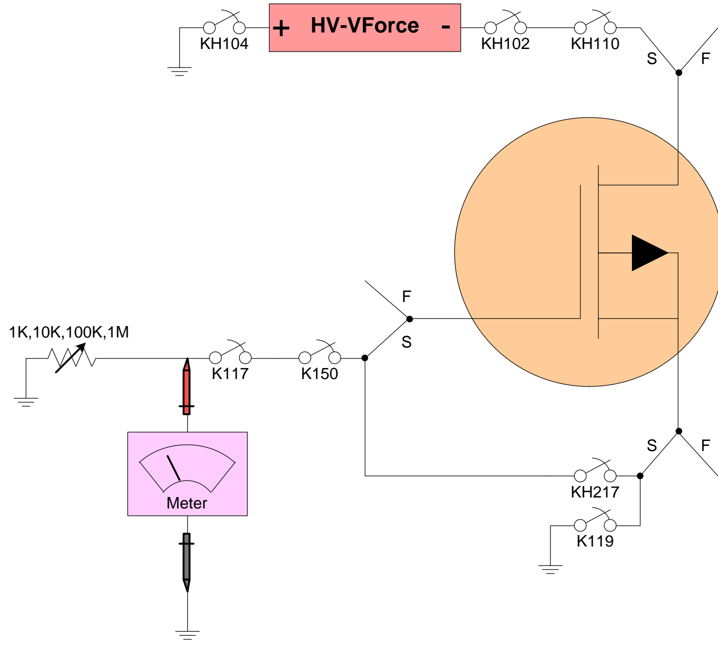
Configuration for P-Channel device using HV supply.



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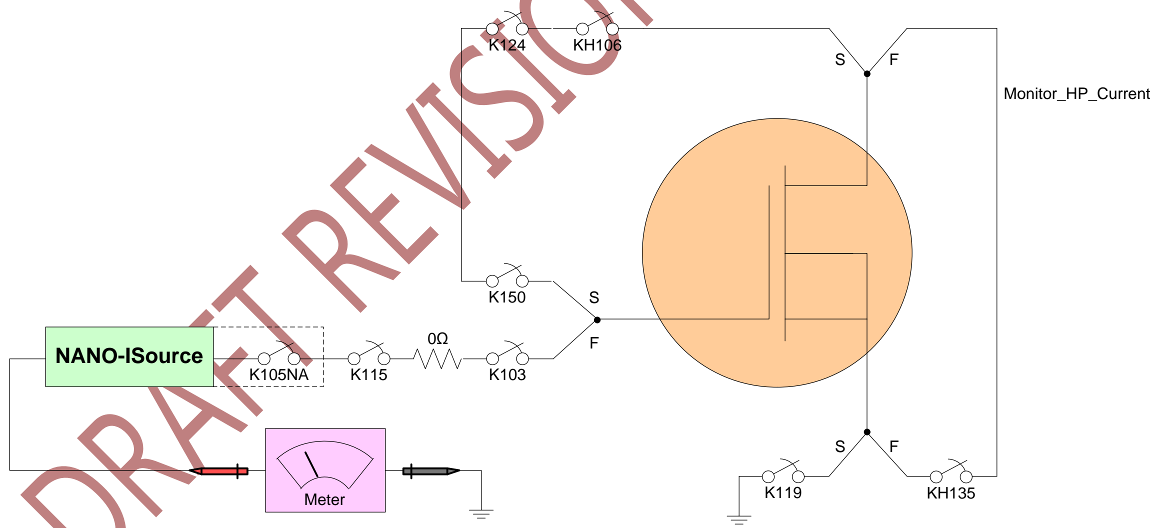
Configuration for N-Channel or P-Channel device using Nano supply and Nano-ammeter.



IDSS Test Parameters

IDSS Configuration

Test Method Configuration

Limits	
IDSS_Max	**IDSS_Max**
IDSS_Min	**IDSS_Min**
Setup	
VDS	100
Z_SuperUser	
LineAvg	**Off**
PulseWidth	0.015
Samples	10

IDSS_Max ***IDSS_Min***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. These values are dependent upon device specification.
VDS	Amount of voltage to apply from Drain to Source.
LineAvg	Ability to automatically set quantity of samples. Choose appropriate power-line cycle rate. If line averaging is enabled, it will be necessary to adjust *PulseWidth* to accommodate a minimum of one (1) line cycle. Additional *VDS* supply settling time should also be added to the *PulseWidth* time.
PulseWidth	Length of time, in seconds, to apply the voltage pulse. This is variable depending on the component(s) being tested. Adjust until a stable reading is achieved.
Samples	Number of measurement samples. Value is used only if *LineAvg* is **Off**. Sample rate is 11.6usec per sample. If quantity of samples is increased, it may be necessary to increase the *PulseWidth*. Should allow additional *VDS* supply

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	settling time.

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IDSS_LV Test

Overview:

Obsolete test. Use *IDSS*.

IDSS_LV was a means to get more leakage measurement accuracy with VDS voltages less than 25V.

IDSS_LV capability has been incorporated into the *IDSS* test.

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IDSS_UHV Test

Overview:

Similar to the IDSS test, except the IDSS_UHV test uses an external Ultra High Voltage supply to achieve VDS values greater than 1200V.

> **NOTE:** Without external UHV supply, maximum VDS will be dependent on internal HV module version which is typically 1200V.

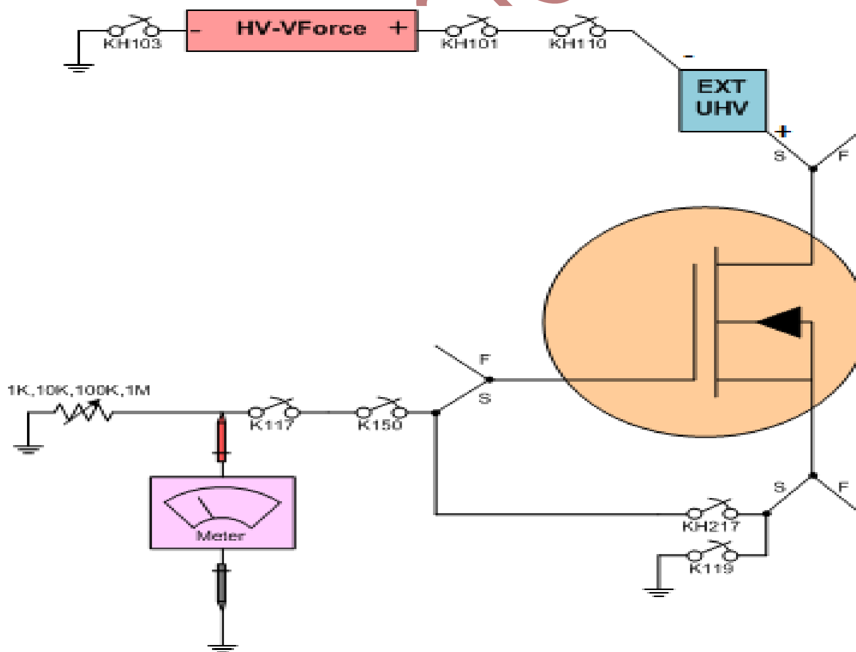
It is suggested to not use the *IDSS_UHV* test for VDS voltages less than or equal to +/-25V. Use the *IDSS* test instead. The HV supply is not as accurate with voltages less than +/-25V.

Description:

The test will set the Gate to *VGS* volts and set the HV supply, and if necessary and available, the UHV supply, to *VDS* volts and measure the leakage current at the end of the test pulse.

IDSS_UHV Test Schematics

Configuration for N-Channel device.



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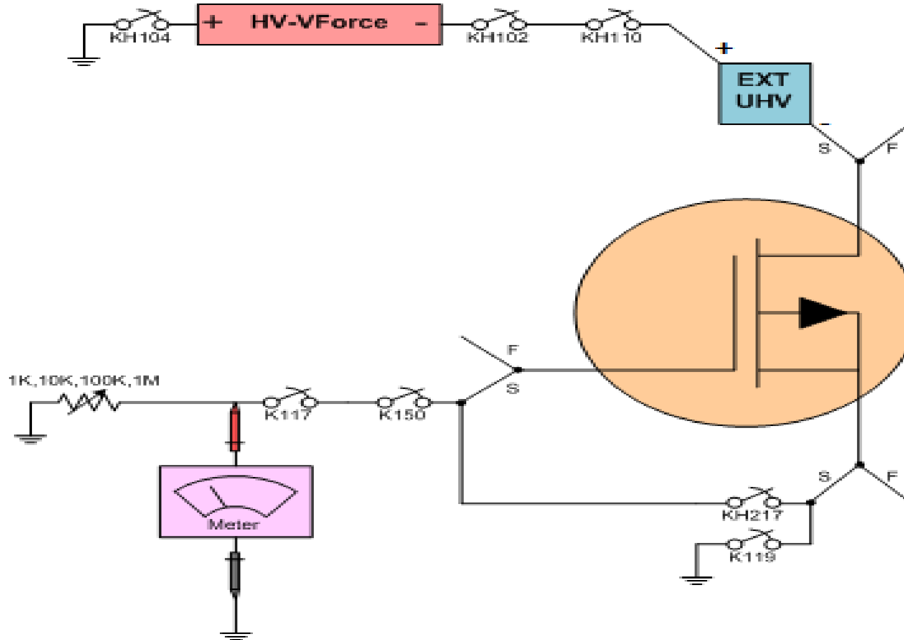
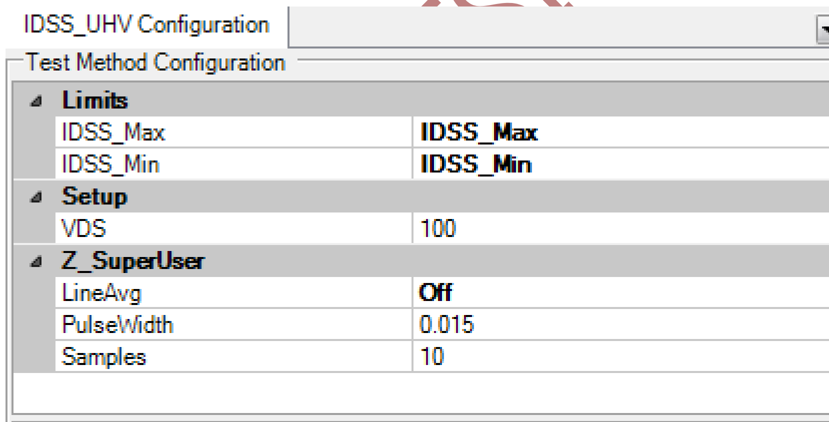
Configuration for P-Channel device.



IDSS_UHV Test Parameters



IDSS_Max ***IDSS_Min***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. These values are dependent upon device specification.
VDS	Amount of voltage to apply from Drain to Source.

LineAvg	Ability to automatically set quantity of samples. Choose appropriate power-line cycle rate. If line averaging is enabled, it will be necessary to adjust *PulseWidth* to accommodate a minimum of one (1) line cycle. Additional *VDS* supply settling time should also be added to the *PulseWidth* time.
PulseWidth	Length of time, in seconds, to apply the voltage pulse. This is variable depending on the component(s) being tested. Adjust until a stable reading is achieved.
Samples	Number of measurement samples. Value is used only if *LineAvg* is **Off**. Sample rate is 11.6usec per sample. If quantity of samples is increased, it may be necessary to increase *PulseWidth*.

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IDSX Test

Overview:

Breakdown voltage or, BVDSS, is the voltage at which the reverse-biased body-drift diode breaks down and significant current starts to flow between the Source and Drain. Typically the Gate to Source voltage will be 0 volts.

Description:

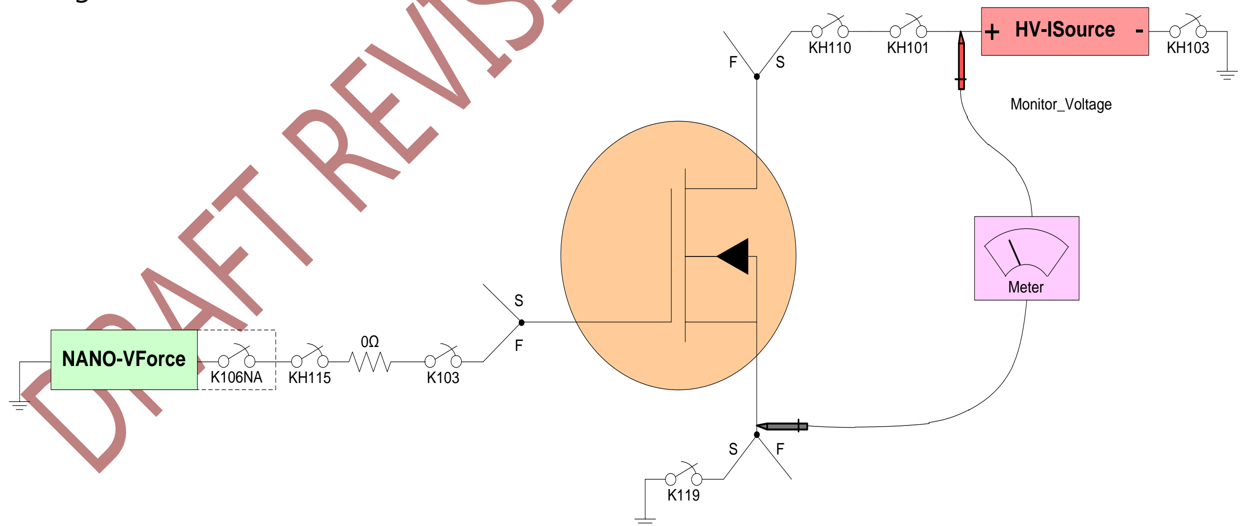
The Drain is connected to the HV current supply. Gate is connected to the Nano VForce supply that can provide a gate voltage of up to +/- 25V.

The test runs by forcing a current (parameter ID - typically 250uA) into the drain pin, forcing a Gate voltage (parameter VGS), and measuring the breakdown voltage (reported by the HVISOURCE to the measurement meter) that happens.

The max limit is optional (use NaN if maximum limit is not desired), but there must be a minimum limit.

IDSX Test Schematics

Configuration for N-Channel device.



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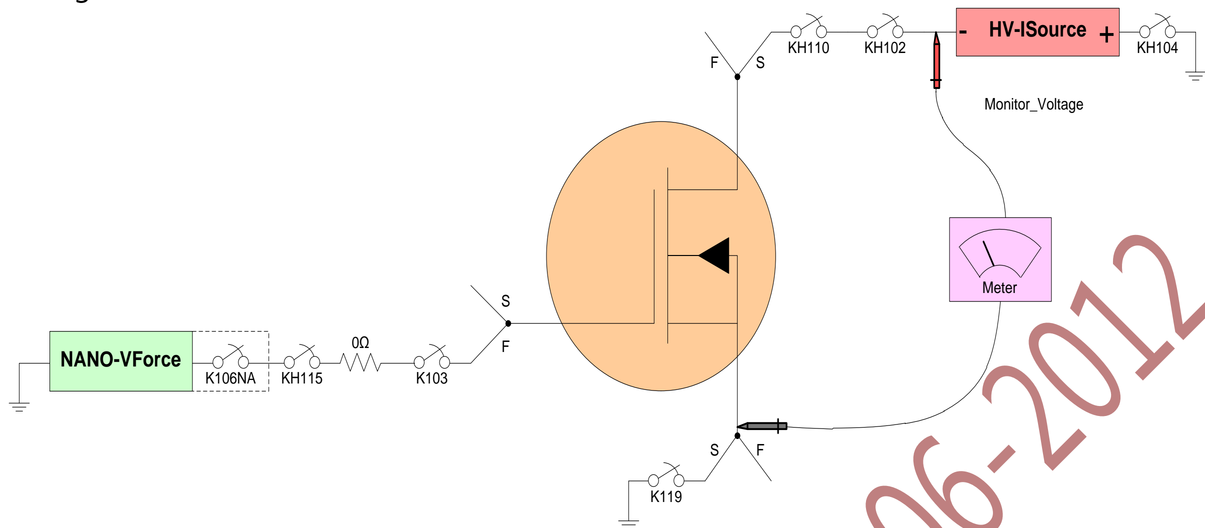
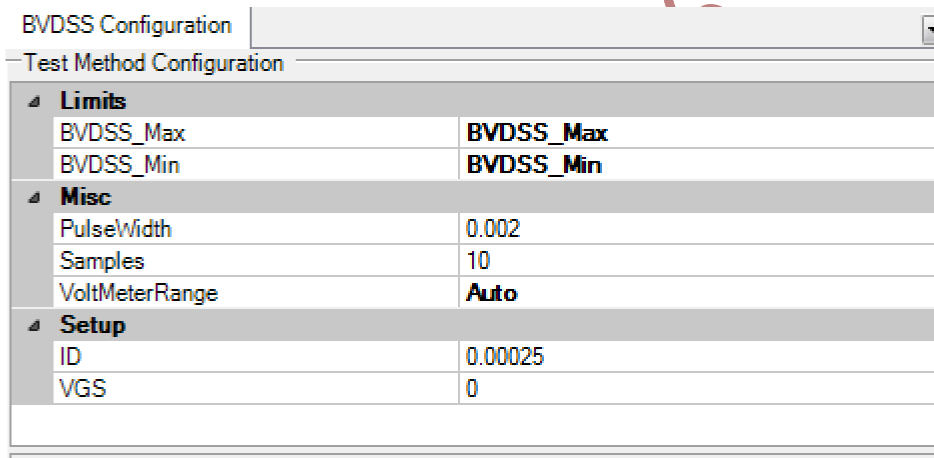
Configuration for P-Channel device.



IDSX Test Parameters



BVDSS_Max ***BVDSS_Min***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. These values define the upper and lower limits of the break-down voltage result.
Pulse width	Length of time in seconds to apply voltage. This must be set long enough for the power to rise fully. With longer cables, or coaxial cables going to a prober, extra time will need to be used, especially with higher voltage devices. So the pulse width must be increased until a stable reading is reached.

Samples	Number of measurement samples to average result. Sample rate is 11.6usec per sample. Ten (10) is normally adequate, but at lower currents, or with more noise, more samples may be required. If the number of samples is increased, *PulseWidth* may need to be increased to match. For example 100 samples would take 1.16msec, so with the default *PulseWidth* of 2msec, this only allows 0.84 msec for the voltage to stabilize, which would be enough for low voltages, but above 100V this would probably mean that the voltage had not settled, and so the first few samples would skew the accuracy of the reading. If you try to reduce *PulseWidth* so that it is less than the time required to make the measurements, the software will generate an alarm each time the test runs. Measurement samples are taken at the end of the pulse.
VoltMeterRange	Provide means to force a voltage measurement range. Default automatically picks range based on *BVDSS_Max*. If *BVDSS_Max* is NaN, then range is determined by *BVDSS_Min* + 300. If the range is less than the break-down voltage, the reported voltage will be the maximum result provided by the range.
ID	Current to apply across Drain-Source.
VGS	Voltage to apply to Gate during break-down test.

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IGSS Test

Overview:

Gate to Source (and optionally Source to Gate) leakage test.

> **NOTE:** For *VGS* and *VGSR* less than or equal to +/-25V, suggest using *ISGS* test. It typically will perform low leakage measurements faster than the *IGSS* test.

Description:

If *VGS* is not 0, apply *VGS* volts to Gate and measure current output of *VGS* supply.

If *VGSR* is not 0, apply *VGSR* volts to Gate and measure current.

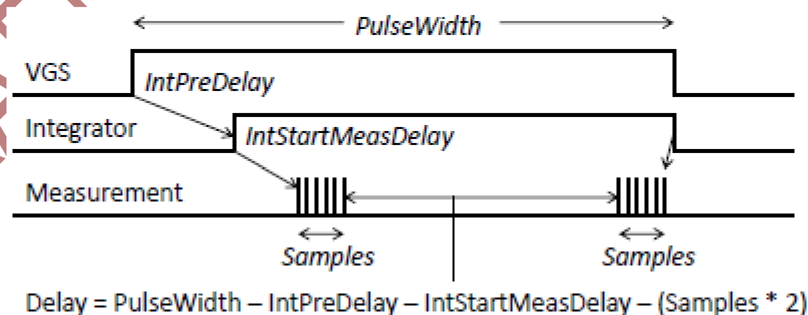
The voltage supply used and measurement accuracy is dependent on the *VGS* (or *VGSR*) value. *VGS/VGSR* voltages greater than +/-25V will use the HV supply. The HV supply minimum current measurement range is 10uA, which is not very accurate for leakage measurements less than 100na.

Integration measurement method:

This test provides the ability to perform an integration leakage measurement methodology (*VGS* less than or equal to +.-25V). This method is typically able to quickly measure very small leakage levels.

The integration measurement method makes two (2) sets of measurements that define a slope. The slope is then used to compute the leakage.

The integration measurement is composed of several variables as shown in the following diagram:



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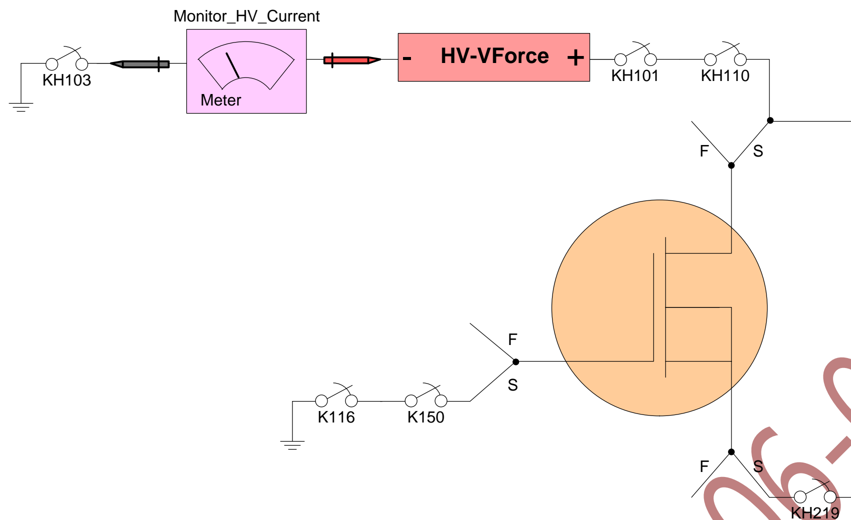
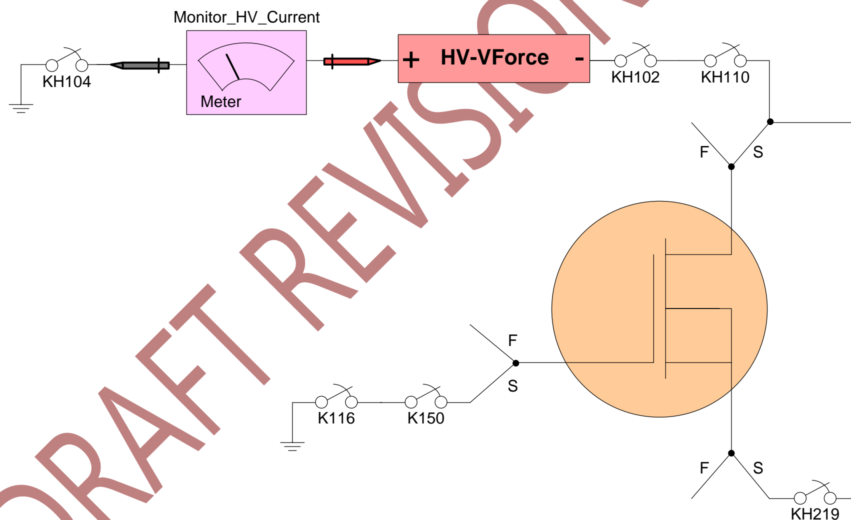
IGSS (and IGSSR) Test Schematics

VGS configuration for N-Channel or P-Channel devices using HV supply.



VGSR configuration for N-Channel or P-Channel devices using HV supply.



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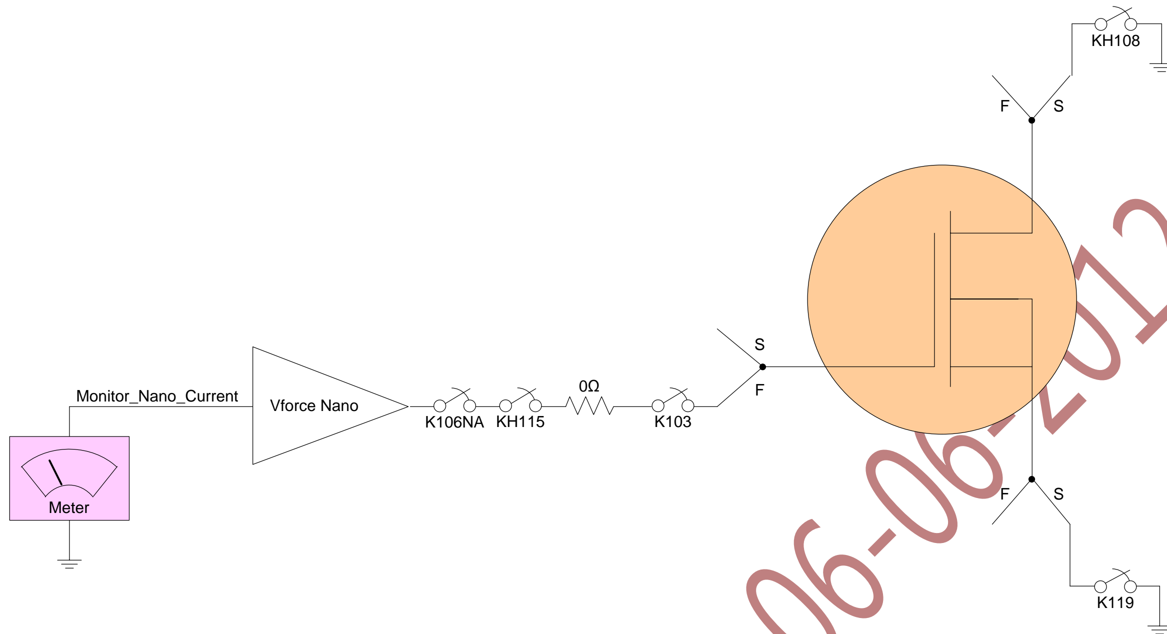
VGS and *VGSR* configuration for N-Channel or P-Channel devices using Nano VForce supply.



IGSS Test Parameters

IGSS Configuration

Test Method Configuration

Parameter	Value
Limits	
IGSS_Max	**IGSS_Max**
IGSS_Min	**IGSS_Min**
IGSSR_Max	**IGSSR_Max**
IGSSR_Min	**IGSSR_Min**
Setup	
VGS	20
VGSR	0
Z_SuperUser	
IntPreDelay	0.0005
IntStartMeasDelay	0.001
LineAvg	**Off**
MeasRange	**Off**
PulseWidth	0
Samples	10

IGSS_Max ***IGSS_Min***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields.

	These values are dependent upon device specification. Defines IGSS (associated with *VGS*) limits.
IGSSR_Max ***IGSSR_Min***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. These values are dependent upon device specification. Defines IGSSR (associated with *VGSR*) limits.
VGS	Gate source voltage, positive value forces positive gate voltage. Negative value forces negative gate voltage. A value of 0 will not perform this phase of the test. Results of this Gate voltage use the *IGSS_Max* and *IGSS_Min* limits.
VGSR	Gate source voltage, positive value forces positive gate voltage. Negative value forces negative gate voltage. A value of 0 will not perform this phase of the test. Results of this Gate voltage use the *IGSSR_Max* and *IGSSR_Min* limits.
IntPreDelay	Integration measurement method that can often accomplish a very low leakage measurement in a shorter time period. Defines the amount of delay after *VGS* (or *VGSR*) is applied before enabling the integrator measurement circuitry. This delay is used to allow the Gate supply to settle before enabling the integration measurement circuitry. If the supply is not properly settled before enabling the measurement circuitry, the effect could be inaccurate measurement or require longer measurement time.
IntStartMeasDelay	Integration measurement method. Defines the amount of delay after the integrator measurement circuitry is enabled to the time of the first set of measurement samples.
LineAvg	Ability to automatically set quantity of samples.

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	Choose appropriate power-line cycle rate. If line averaging is enabled, it will be necessary to adjust *PulseWidth* to accommodate a minimum of one (1) line cycle. Additional *VGS* supply settling time should also be added to the *PulseWidth* time. If using integration measurement method, it is suggested to turn *LineAvg* **Off**.
MeasRange	Ability to force a specific leakage current range. The range normally is based on the *IGSS_Max* or *IGSSR_Max* limit (when *MeasRange* = **Off**). The 100na range can be used to measure current values as high as 350na. The automatic selection would use the 1ua range. Forcing the range of 100na would produce a more accurate measurement, especially if the typical DUT leakage is less than 10na.
PulseWidth	Length of time, in seconds, to apply the *VGS* (or *VGSR*) voltage pulse. This is variable depending on the component(s) being tested. Adjust until a stable reading is achieved. If using integration measurement method, *PulseWidth* must be long enough for two (2) times the quantity of samples, plus *IntStartMeasDelay*, plus *IntPreDelay*. Any additional time that is left over is what defines the delay between the first set of measurement samples and the second set of measurement samples.
Samples	Number of measurement samples. Value is used only if *LineAvg* is **Off**. Sample rate is 11.6usec per sample. If quantity of samples is increased, it may be necessary to increase the *PulseWidth*. Should allow additional *VDS* supply settling time.

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ISGS Test

Overview:

Source to Gate (and optionally Gate to Source) leakage test.

NOTE: This test is limited to +/-25V. Suggest using *IGSS* test for voltages greater than +/-25V.

Description:

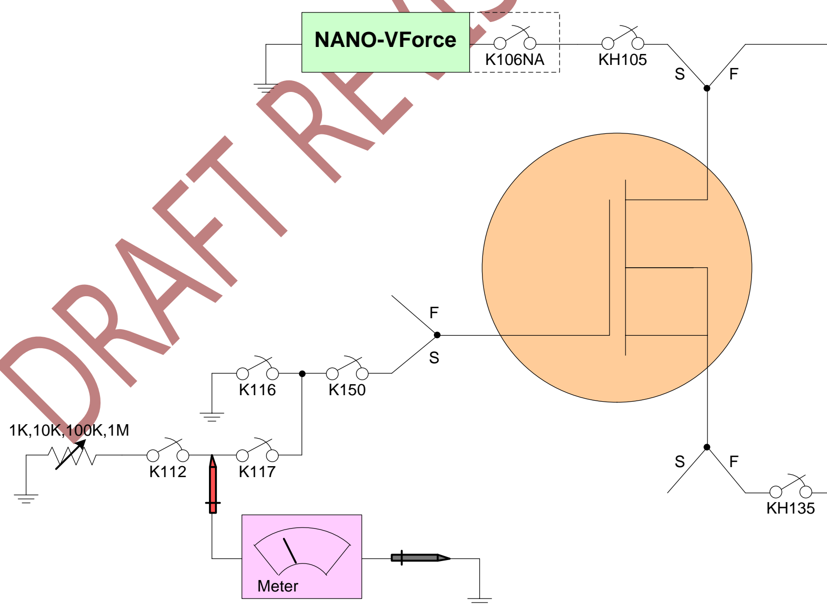
The Gate pin is tied to ground through a current sense resistor.

First close relays including K116, then measure calibration voltage across the current sense resistor. K116 is then opened and voltage applied to the Drain and Source pins and voltage is measured across the current sense resistor.

Current is computed as (vLeakage – vCal) / Rsense.

ISGS Test Schematic

VGS and VGSR condition for N-Channel or P-Channel devices.



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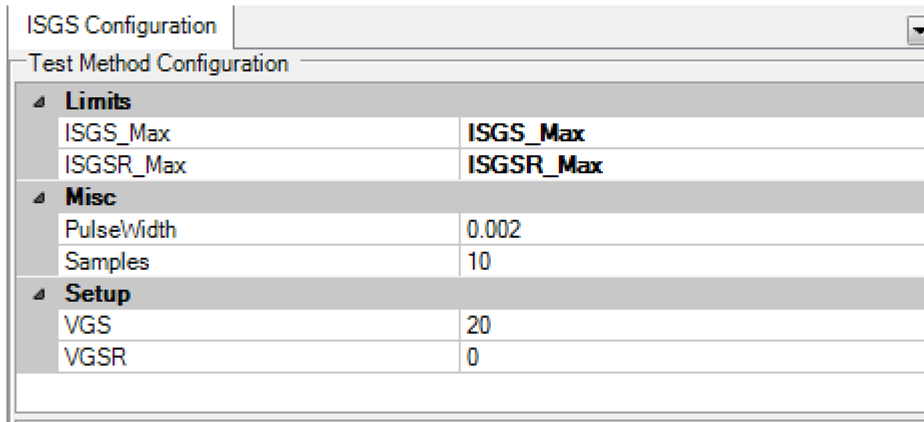
ISGS Test Parameters



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ISGS_Max	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. These values are dependent upon device specification. Defines maximum limit of *VGS* condition.
ISGSR_Max	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. These values are dependent upon device specification. Defines maximum limit of *VGSR* condition.
PulseWidth	Length of time in seconds to apply each voltage pulse. This is variable depending on the component(s) being tested. Adjust the pulse width until a stable reading is achieved.
Samples	Number of measurement samples. Sample rate is 11.6usec per sample. If the quantity of samples is increased, may need to increase the *PulseWidth* accordingly.
VGS	A value greater than 0 will place a –*VGS* voltage to the Drain and Source pins (positive voltage to Gate-Source).
VGSR	A value greater than 0 will place a +VGSR voltage to the Drain and

	Source pins (negative voltage to Gate-Source).

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KELVIN Test

Overview:

Test that the device is making good contact with socket, handler, or probe pins.

ConnectionTest test provides a fixed quantity of logged results and is limited to 25mA test current. Voltage limited to +10V at DUT pins.

CONTINUITY test performs the same series summed resistance but will not break the resistance down into the three components of Gate, Drain, and Source. *CONTINUITY* uses a fixed 25mA forcing current. Voltage is limited to +36V at DUT pins.

KELVIN test quantity of logged results can vary, depending on the series summed resistance and other settings. *KELVIN* is limited to 100mA test current. Voltage is limited to +10V at the DUT pins.

Description:

Measure the series Gate, Drain, and Source Force/Sense resistance path. If resistance goes above a threshold value defined by *RKELVIN_MAX * 60%* (or *EngMode* is true) and if *I_Apply* is 25ma or less, measure and log each Gate, Drain, and Source contact resistances separately.

If *I_Apply* is 100ma, will measure and log only the series summed measurement.

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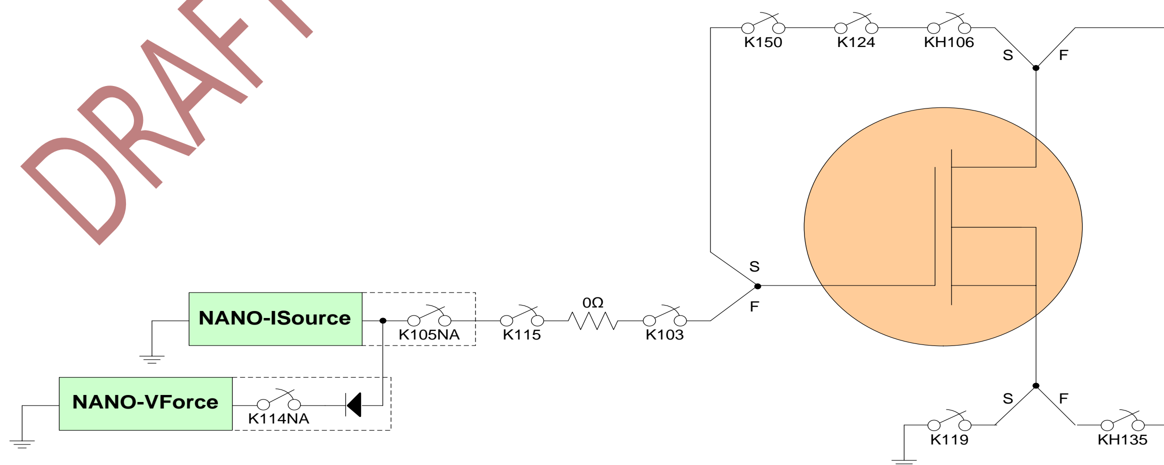
KELVIN Test Schematics

Condition for Gate, Drain, and Source path with N-Channel or P-Channel devices.



Condition for Gate contact resistance measurement.

Condition for Drain contact resistance measurement.

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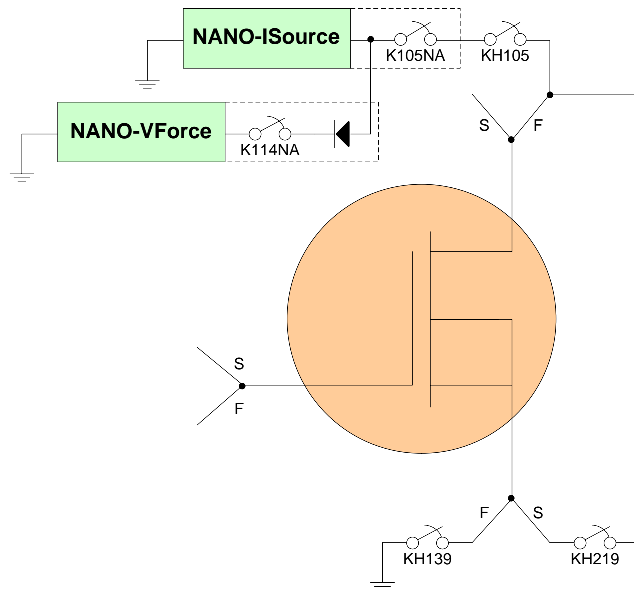
Condition for Source contact resistance measurement.



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KELVIN Test Parameters

KELVIN Configuration

Test Method Configuration

Limit	
RKELVIN_MAX	**RKELVIN_MAX**
Misc	
EngMode	False
I_Apply	**R25mA**
PulseWidth	0.0003
Samples	5

RKELVIN_MAX	Parameter is defined on the *Program Variables* tab or can be changed by directly typing the values in the fields.
EngMode	Enables logging of additional data (and current or voltage information as part of the log description). If *I_Apply* is R100mA and *EngMode* is True, will not log separate Gate, Drain, and Source contact resistances.

I_Apply	Amount of current to apply.
PulseWidth	Length of time, in seconds, to apply each current pulse. Adjust the pulse (ramp up the length) until a stable reading is achieved.
Samples	Number of samples to average for measurement result. Sample rate is 11.6usec per sample. If *Samples* is increased, may have increase *PulseWidth* accordingly.

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LATCH Test

Overview:

Test device for latch-up condition.

Description:

Apply *VGS* to Gate, then apply *ID* for 500us, set Gate to 0V for 10ms, set Gate to *VGS* for 500us, measure ID current, set Gate to 0V and remove ID.

If measured ID is less than or equal to half of *ID* parameter, will fail with a logged value of 1.

If measured ID is greater than half of *ID* parameter, will pass with a logged value of 0.

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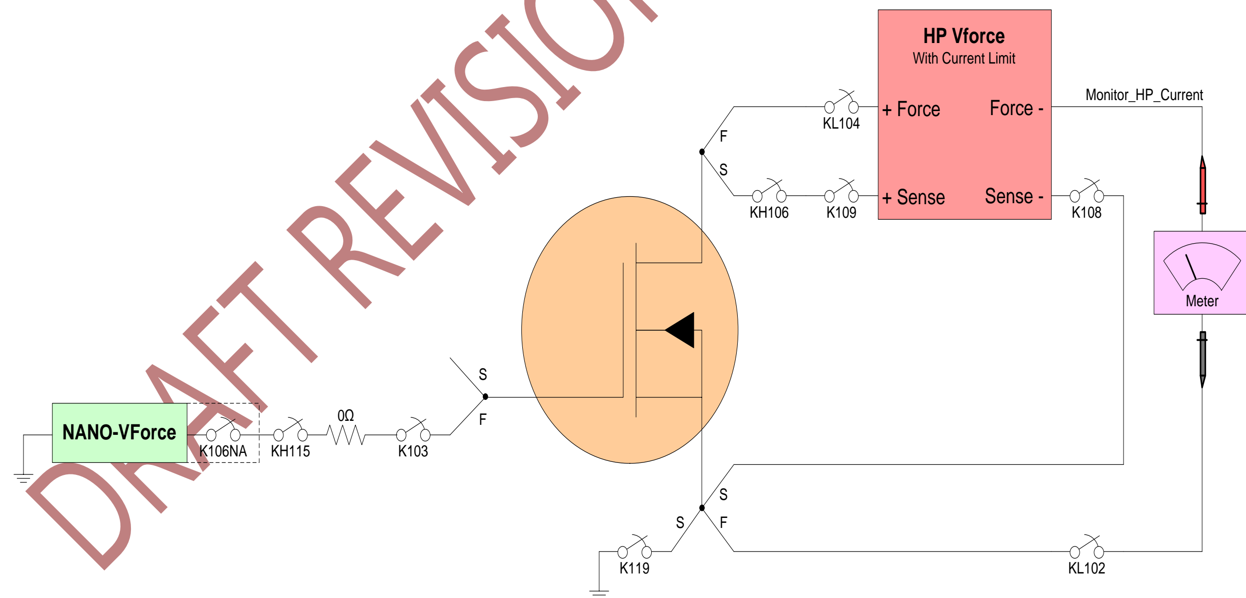
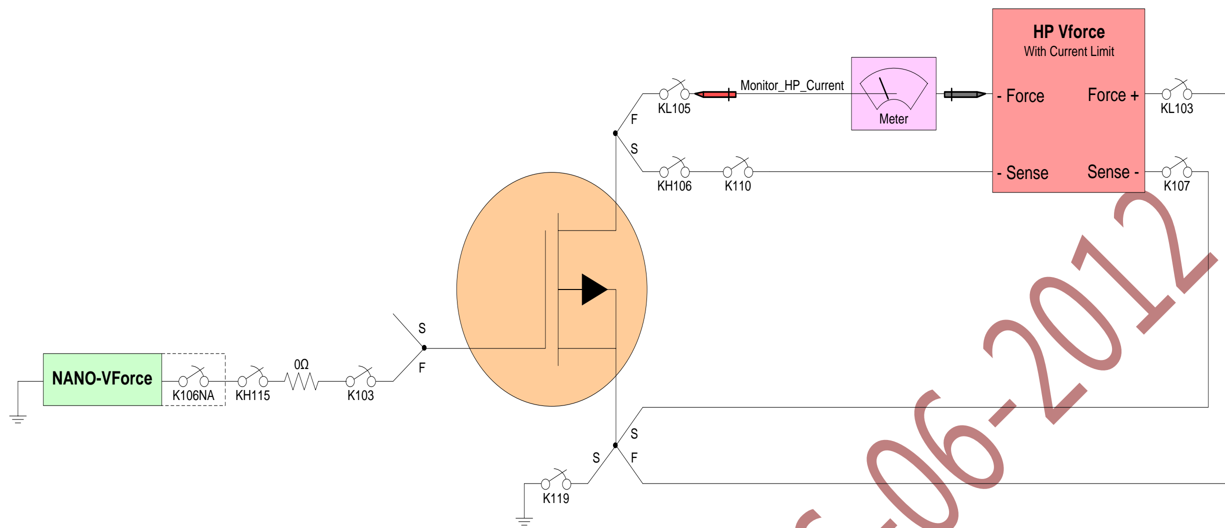
LATCH Test Schematics

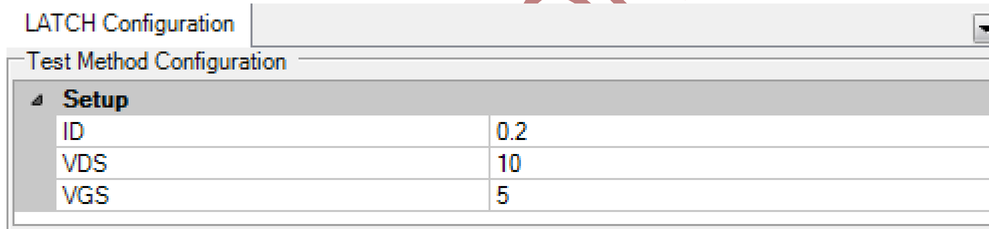
Condition for N-Channel device.



Condition for P-Channel device.



LATCH Test Parameters



ID	Amount of current, in amps, to apply across Drain-Source.
VDS	Drain-Source voltage limit.
VGS	Gate voltage to apply.

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OpenShort Test

Overview:

A method to detect if device pins, or pads, are making contact with the socket, handler, or prober pins.

Description:

The *OpenShor*t test is effectively a VGS test (with Gate and Drain tied together).

Apply *ID* current from Gate and Drain to Source and measure voltage from Drain to Source.

If the measured voltage exceeds the *OpenShortMax* limit, the DUT and/or contacts are open. If the measured voltage is less than the *OpenShortMin* limit, the DUT is shorted.

NOTE: This test is not as thorough as the *CONTINUITY* or *KELVIN* tests.

For currents less than or equal to 25mA, the *OpenShort* test only checks connectivity of the Drain-Sense, Source-Sense, and Gate-Force tester ports to the DUT.

For currents greater than 25mA, the *OpenShort* test forces current through the tester Drain-Force and Source-Force ports, and measures on Drain-Sense and Source-Sense ports. The Gate-Force tester port is the only Gate to DUT connection tested.

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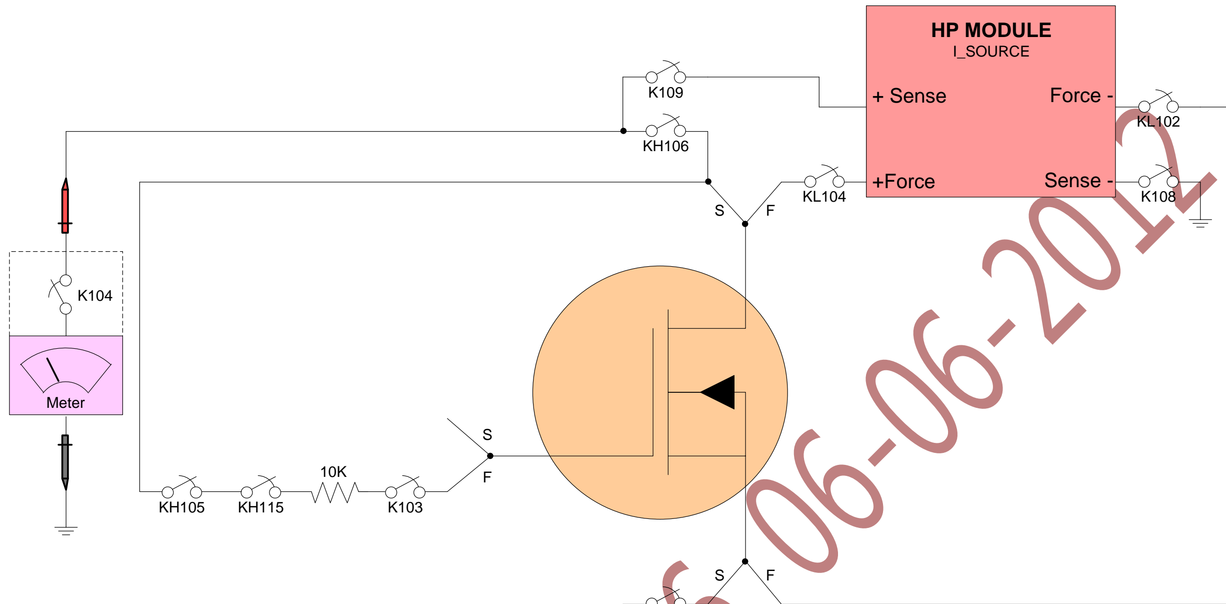
OpenShort Test Schematics

Condition for N-Channel device using HP supply.



Condition for P-Channel device using HP supply.

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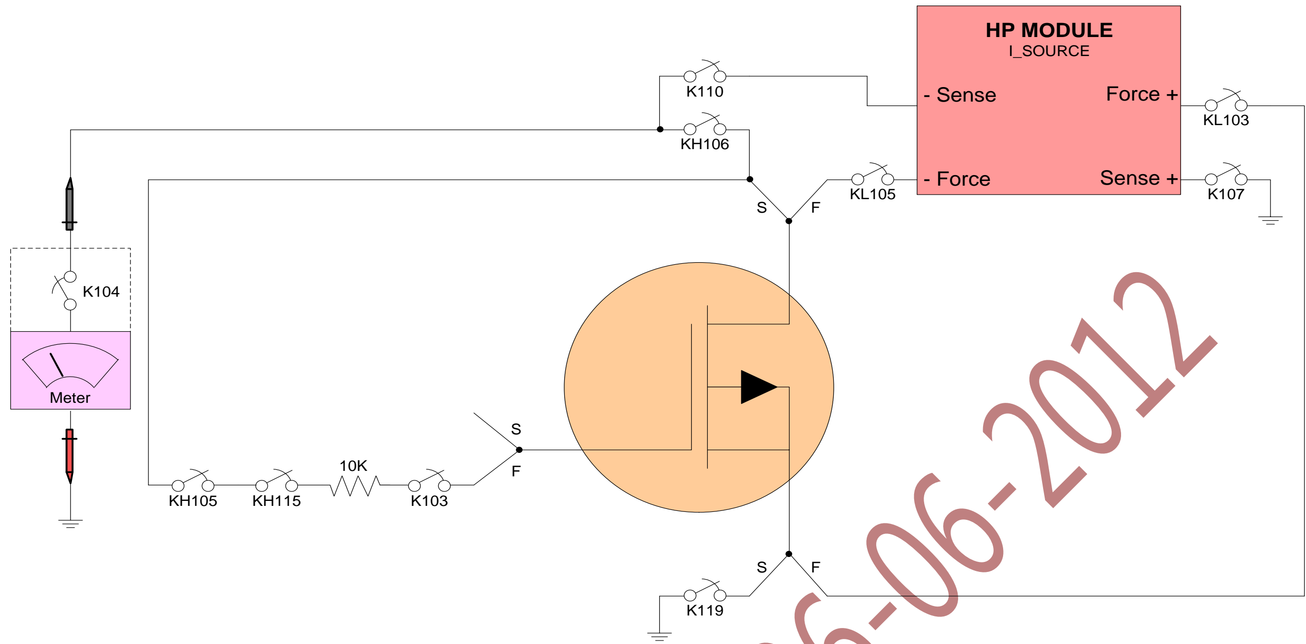
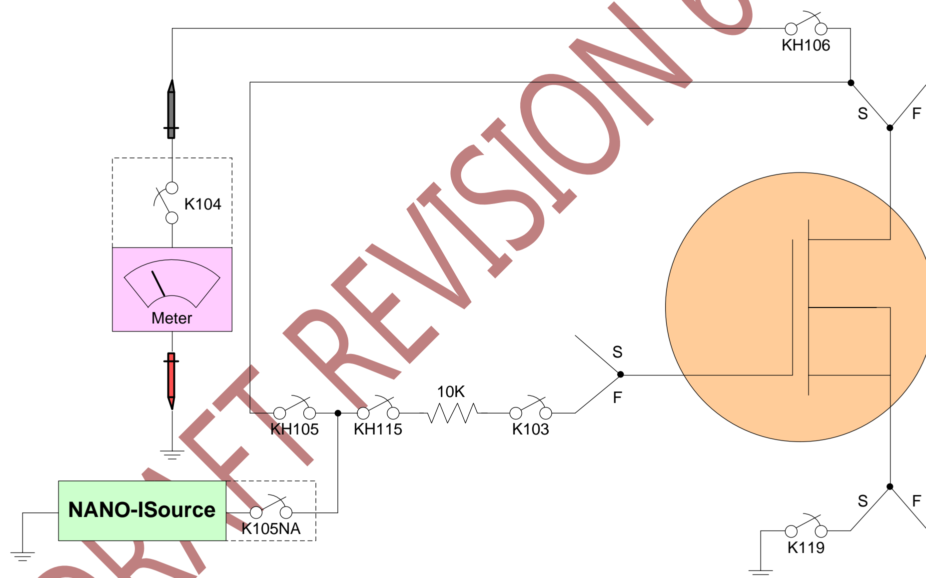


Condition for N-Channel or P-Channel devices using Nano VForce supply.



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OpenShort Test Parameters

OpenShort Configuration

Test Method Configuration

Limit	
OpenShortMax	**OpenShortMax**
OpenShortMin	**OpenShortMin**
Misc	
PulseWidth	0.003
Samples	10
Setup	
ID	0.005
VDS	10

OpenShortMax ***OpenShortMin***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. These values are dependent upon device specification. *OpenShortMax* should be between *VDS* and *OpenShortMin* limit values. *OpenShortMin* limit should be between 0 and *OpenShortMax* limit value.
PulseWidth	Length of time, in seconds, to apply the current pulse. This is variable depending on the component(s) being tested and *ID* current applied. Adjust the pulse (ramp up the length) until a stable reading is achieved.
Samples	Number of samples to average for measurement result. Sample rate is 11.6usec per sample. If *Samples* is increased, may need to increase *PulseWidth* accordingly.
ID	Drain-Source current to apply.
VDS	Current source supply is used for the test. This value will

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	limit the Drain-Source voltage the supply is allowed to generate if there is an open condition.

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RDSON Test

Overview:

Measure the resistance of Drain-Source with the device on.

> Use *RDSON_Cal* test for Golden Unit offset testing methodology. Other than Golden Unit offset, there is no functional difference from the *RDSON_Cal* test.

Description:

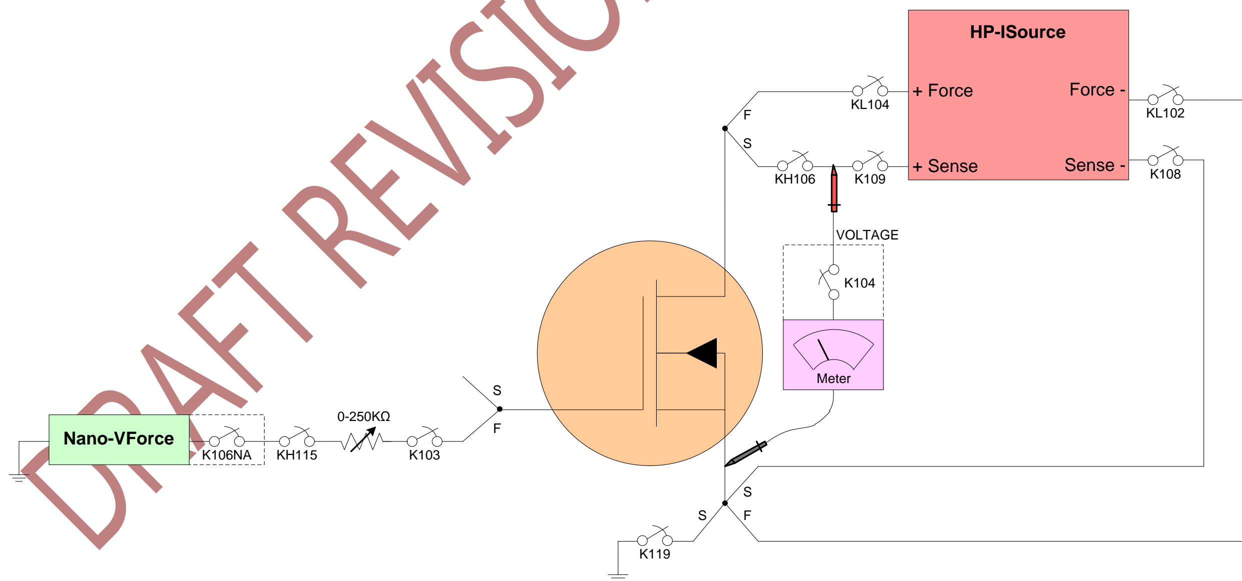
Apply Gate voltage VGS and Drain-Source current ID and measure voltage across Drain-Source.

Resistance is computed from applied current and measured voltage.

Voltmeter offset is removed by performing a calibration measurement prior to the test pulse.

RDSON Test Schematics

Condition for N-Channel device.



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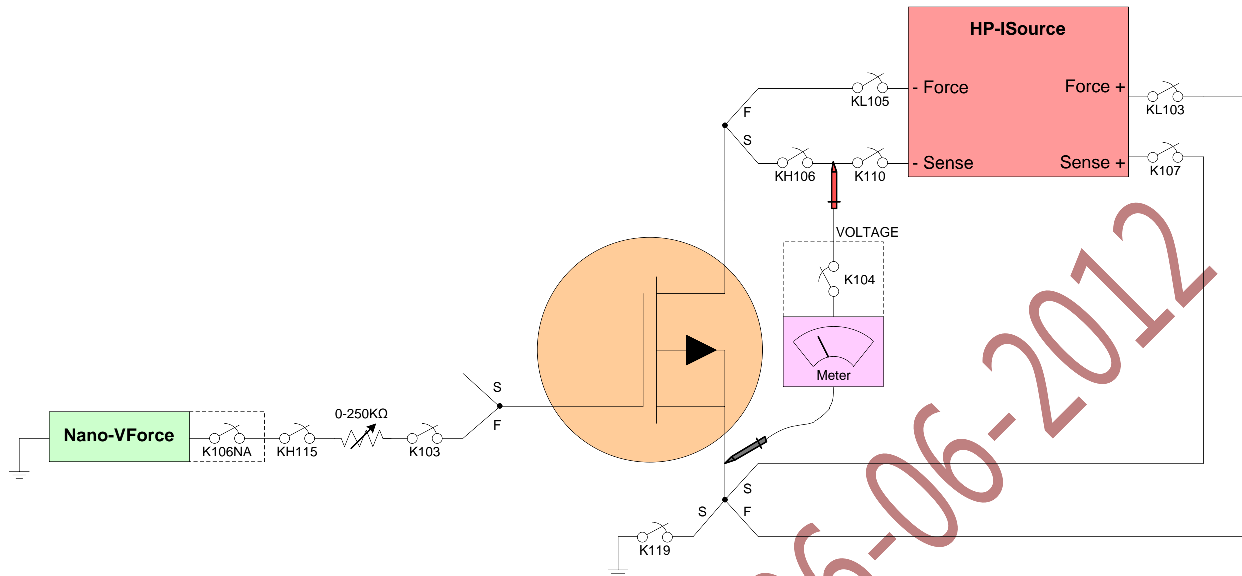
Condition for P-Channel device.



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RDSON Test Parameters

RDSON Configuration

Test Method Configuration

Parameter	Value
Limits	
RDSON_Max	**RDSON_Max**
RDSON_Min	**RDSON_Min**
Misc	
PulseWidth	0.0005
Samples	5
Setup	
ID	10
VGS	10
SuperUser	
CurrentRange	**RangeAuto**
DisconnectSense	False
GateRes10K	False

RDSON_Max ***RDSON_Min***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields.

	These values are dependent upon device specification. RDSON_Min value can be NaN (or None).
PulseWidth	Length of time, in seconds, to apply the current pulse. This is variable depending on the component(s) being tested. Adjust the pulse (ramp up the length) until a stable reading is achieved.
Samples	Number of samples to average for measurement result. Sample rate is 11.6usec per sample. If *Samples* is increased, may need to increase *PulseWidth* accordingly.
ID	Amount of current, in amps, to apply during the test.
VGS	Amount of voltage to apply to the Gate during the test.
CurrentRange	This parameter provides a method to override the current source automatic selection method. One situation for forcing a range is if the current is on the current sourcing instrument boundary condition. Sitting current on one range versus another may produce more accurate results. Note that the automatic mode will always use the same range during testing for any given *ID* value is changed during the test.
DisconnectSense	Set True to disconnect high power instrument voltage sense. For most situations, more accuracy can be obtained by setting *DisconnectSense* to True. Some versions of the RDSON test will always disconnect the current source Sense, therefore this parameter has no affect.

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GateRes10K	Set True to enable 10K Ohm resistor in series with the DUT Gate. Set False for no DUT Gate series resistance (other than the normal instrument system resistance). If a DUT oscillates during the Rdson test, often the oscillation can be eliminated by adding series Gate resistance. Note however, that this can slow down the DUT response time, therefore *PulseWidth* may have to be increased.

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RDSON_Cal Test

Overview:

Measure the resistance of Drain-Source with the device on.

This test is typically used for Golden Unit offset testing methodology. This test can also be used for normal testing which does not rely on Golden Unit offset. Other than Golden Unit offset, there is no functional difference from the *RDSON* test.

Description:

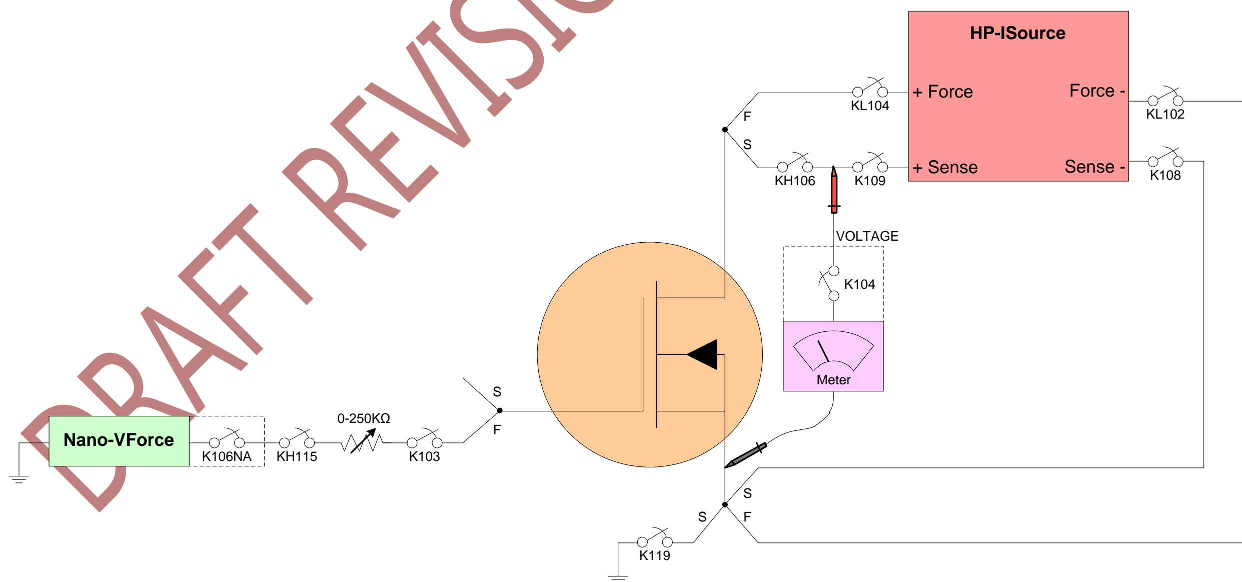
Apply Gate voltage VGS and Drain-Source current ID and measure voltage across Drain-Source.

Resistance is computed from applied current and measured voltage.

Voltmeter offset is removed by performing a calibration measurement prior to the test pulse.

RDSON_Cal Test Schematics

Condition for N-Channel device.



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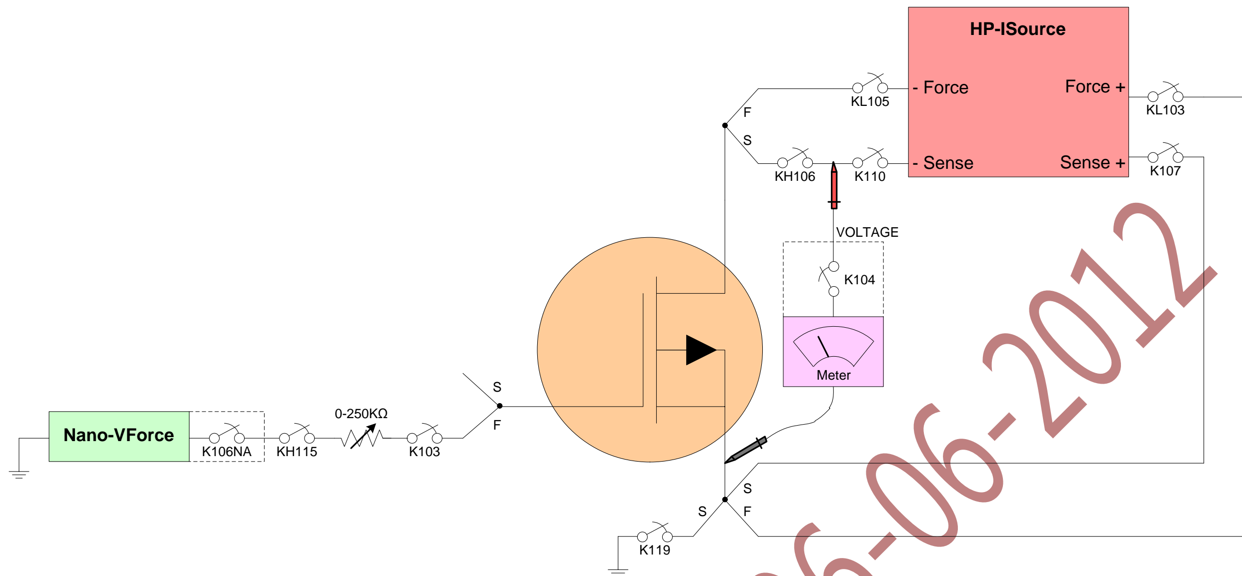
Condition for P-Channel device.



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RDSON_CAL Test Parameters

RDSON_Cal Configuration

Test Method Configuration

Parameter	Value
GDCAL	
CalUnitMeasvalue_Max	10
CalUnitMeasvalue_Min	0
Offset_Max	10
Offset_Min	-10
Limits	
RDSON_Max	**RDSON_Max**
RDSON_Min	**RDSON_Min**
Misc	
PulseWidth	0.0005
Samples	5
Setup	
ID	10
VGS	10
SuperUser	
CurrentRange	**RangeAuto**
DisconnectSense	False
GateRes10K	False

CalUnitMeasValue_Max ***CalUnitMeasValue_Min***	Minimum and Maximum limits when measuring Golden Unit device.
Offset_Max ***Offset_Min***	Minimum and Maximum limits allowed for Golden Unit device offset value. Golden Unit offset is a value that is applied to device testing in order to compensate for tester measurement differences.
RDSON_Max ***RDSON_Min***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. These values are dependent upon device specification. RDSON_Min value can be NaN (or None).
PulseWidth	Length of time, in seconds, to apply the current pulse. This is variable depending on the component(s) being tested. Adjust the pulse (ramp up the length) until a stable reading is achieved.
Samples	Number of samples to average for measurement result. Sample rate is 11.6usec per sample. If *Samples* is increased, may need to increase *PulseWidth* accordingly.
ID	Amount of current, in amps, to apply during the test.
VGS	Amount of voltage to apply to the Gate during the test.
CurrentRange	This parameter provides a method to override the current source automatic selection method. One situation for forcing a range is if the current is on the current sourcing instrument boundary condition. Sitting current on one range versus another may

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	produce more accurate results. Note that the automatic mode will always use the same range during testing for any given *ID* value is changed during the test.
DisconnectSense	Set True to disconnect high power instrument voltage sense. For most situations, more accuracy can be obtained by setting *DisconnectSense* to True. Some versions of the RDSON test will always disconnect the current source Sense, therefore this parameter has no affect.
GateRes10K	Set True to enable 10K Ohm resistor in series with the DUT Gate. Set False for no DUT Gate series resistance (other than the normal instrument system resistance). If a DUT oscillates during the Rdson test, often the oscillation can be eliminated by adding series Gate resistance. Note however, that this can slow down the DUT response time, therefore *PulseWidth* may have to be increased.

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SingleEventBias Test

Overview:

Monitor and plot IDSS and IGSS over a period of time.

This test is typically used to monitor DUT IDSS and IGSS during ion bombardment.

Description:

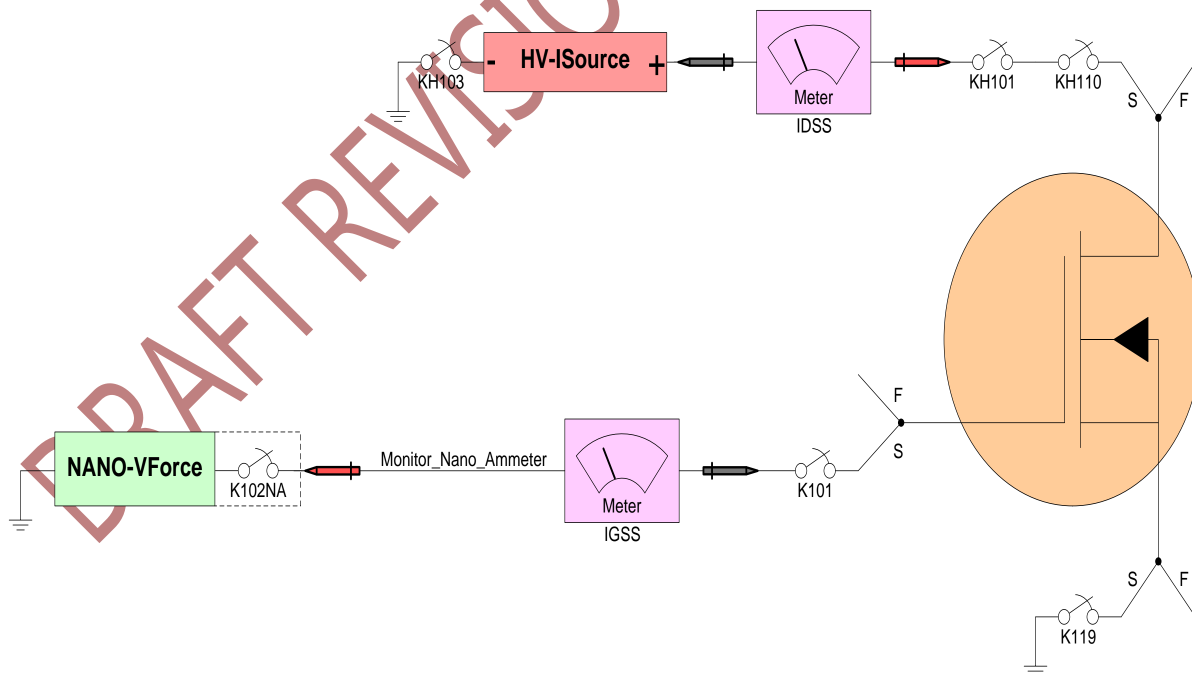
Apply Gate voltage *VGS* and Drain-Source voltage *VDS* for approximately *RunTime* seconds.

During the *RunTime* period, the test will continuously measure and graphically plot the IDSS and IGSS results. The measurement sample rate is approximately *SampleTime* per sample.

The graphic display form **Stop Test** button provides ability to terminate the test loop.

SingleEventBias Test Schematics

Condition for N-Channel device.



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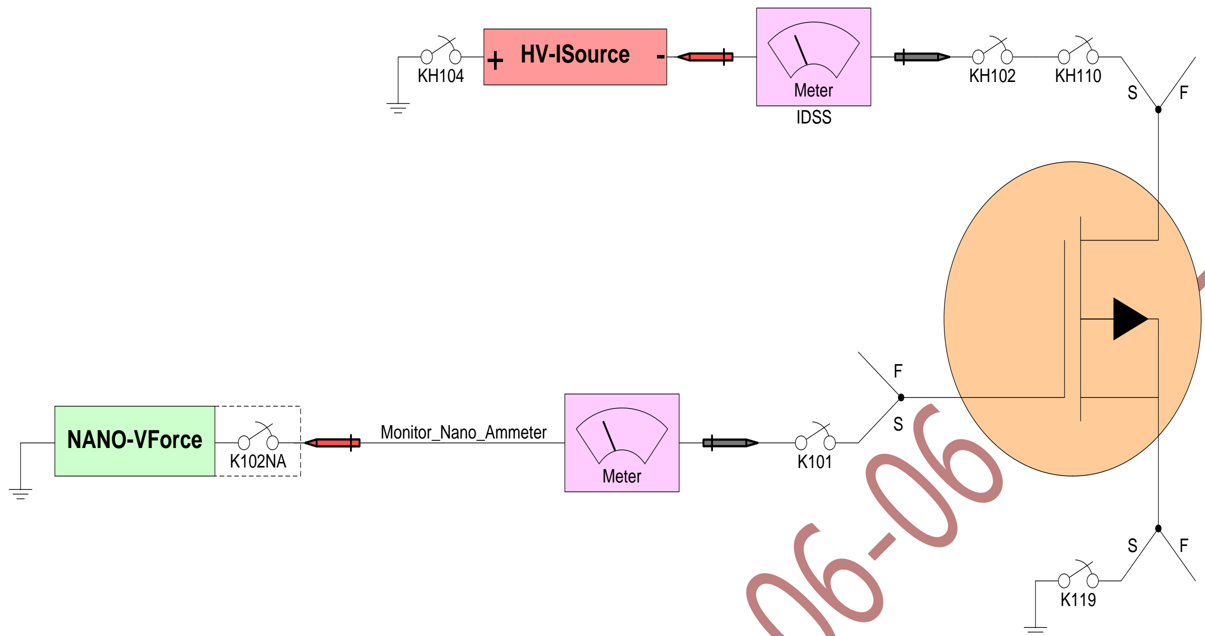
Condition for P-Channel device.



SingleEventBias Test Parameters

SingleEventBias Configuration

Test Method Configuration

Parameter	Value
Limits	
IDSS_Max	**IDSS_Max**
IDSS_Min	**IDSS_Min**
IGSS_Max	**IGSS_Max**
IGSS_Min	**IGSS_Min**
Setup	
RunTime	3
SampleTime	0.1
ThreeWireShort	False
VDS	100
VGS	0

IDSS_Max ***IDSS_Min***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields.

	These values specify the IDSS limits.
IGSS_Max ***IGSS_Min***	These parameters are defined on the Program Variables tab or can be changed by directly typing the values in the fields. These values specify the IGSS limits.
RunTime	Specifies the approximate maximum time to monitor the IDSS and IGSS measurements of the DUT. Note that the test may be premature terminated by pressing the **Stop Test** button on the graphic plot form.
SampleTime	Defines sample rate. Value can be between 8.05msec to 1second. Note that the smaller the value, the faster the points are plotted on the graphic form. The form has a limited quantity of sample storage, meaning old data will be scrolled off the form.
ThreeWireShort	True to connect the Gate, Source, and Drain pins of the DUT together after the test has completed. False will leave the DUT pins floating. **NOTE:** If using an external DUT selection MUX, this option may not make a difference, other than presetting the DUT side of the MUX prior to the MUX changing states. Ideally, the DUT side of the MUX would be capable of shorting each DUT set of pins together.
VDS	Amount of Drain to Source voltage to apply during the test.
VGS	Amount of Gate to Source voltage to apply during the test.

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TRIP_TSN Test

Overview:

Measure specially designed FET trip temperature.

Description:

Since this test logs a temperature, it is suggested to measure Vsd (intrinsic diode voltage) prior to parametric testing while the die is still at ambient temperature. This value is then saved and used as part of the trip temperature that occurs latter in the test flow.

Vsd is measured by placing a small current through the intrinsic diode and measuring the voltage across the diode. The VSD measurement schematic shows the method for Vsd measurement.

The ambient Vsd is measured prior to heating the die. The final Vsd is measured after the die has been heated.

To heat the die, apply *VGS* (Gate voltage) and *VDS* (Drain-Source voltage) voltages. (Refer to the heating pulse schematics below.) The trip test will wait for the first trip condition (ID current less than *ID_Threshold*), or for maximum of *TripTimeout*.

If the FET did not achieve trip condition within the *TripTimeout*, the logged trip temperature will be negated.

If the *DelayAfterTrip* value is greater than 0, the test will continue to apply VGS and VDS for the *DelayAfterTrip* time (plus time for the FET to achieve final trip condition). During this time, the test will monitor the duration of FET ON and OFF times and retain the largest ON and OFF time detected.

If the detected ON time is greater than *dTRIP_MAX_ON* or less than *dTRIP_MIN_ON*, the logged trip temperature will be negated, if not already a negative value.

If the detected OFF time is greater than *dTRIP_MAX_OFF* or less than *dTRIP_MIN_OFF*, the logged trip temperature will be negated, if not already a negative value.

The trip temperature is computed by the following formula:

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Ttrip (°C) = (ABS(Vsd_final – Vsd_ambient) / (*Kfactor* / 1000)) + *Tmb* + *Tadj*.

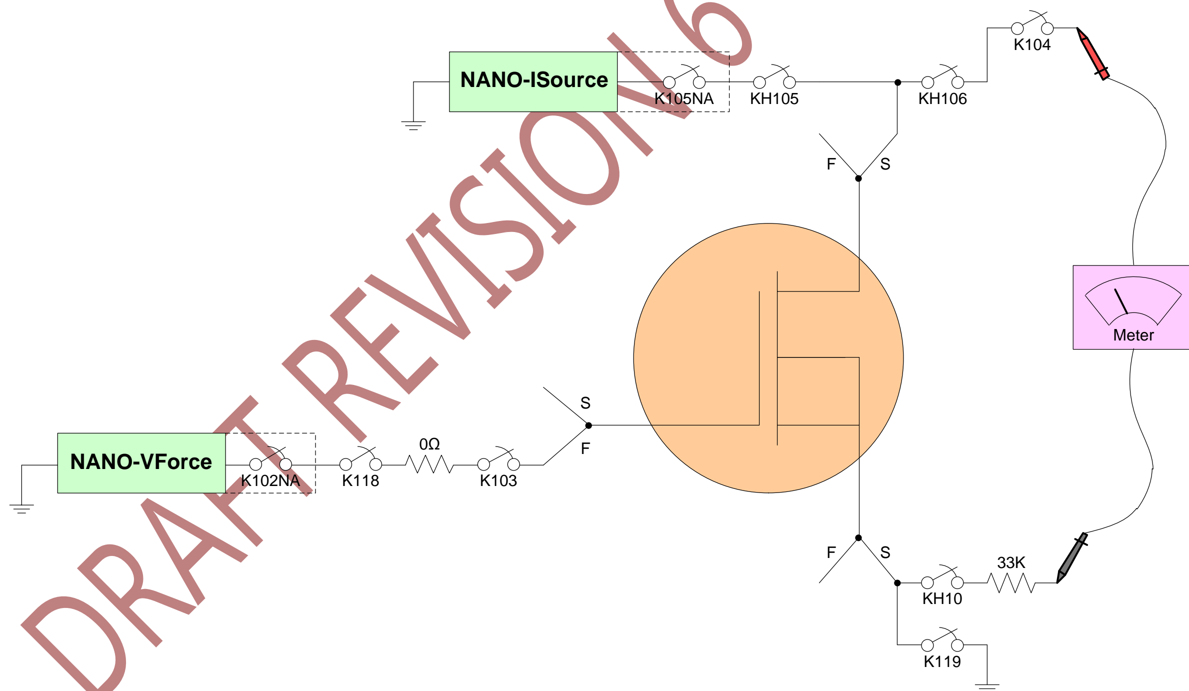
There is a special mode that can produce a *VGS* & *VDS* voltage for a fixed period of time (plus time for FET to achieve final trip condition), no matter when the FET trips. This is accomplished by setting the *DelayAfterTrip* value to exactly 1.23e-6 and setting the *TripTimeout* to the desired pulse width.

During the fixed trip pulse width mode, the test will detect the longest duration of FET ON and OFF times (following first time trip). These times will be tested against the respective limits (as mentioned above).

If the FET did not trip during the fixed pulse width, the temperature will be negated.

TRIP_TSN Test Schematics

Condition for measuring Vsd of N-Channel or P-channel devices.



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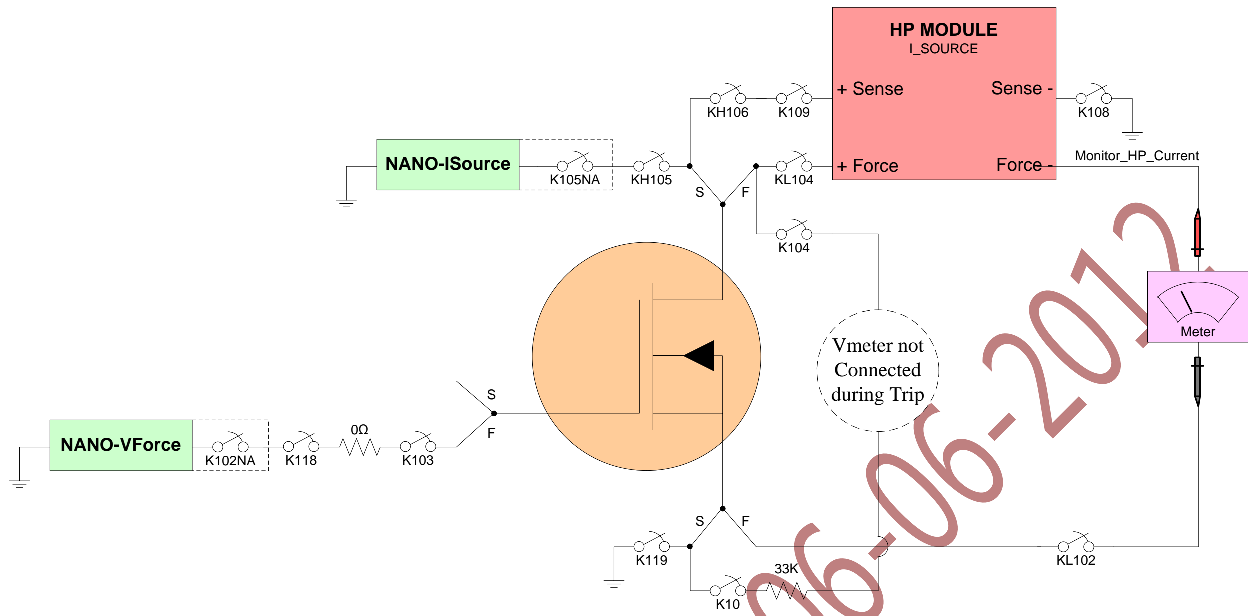
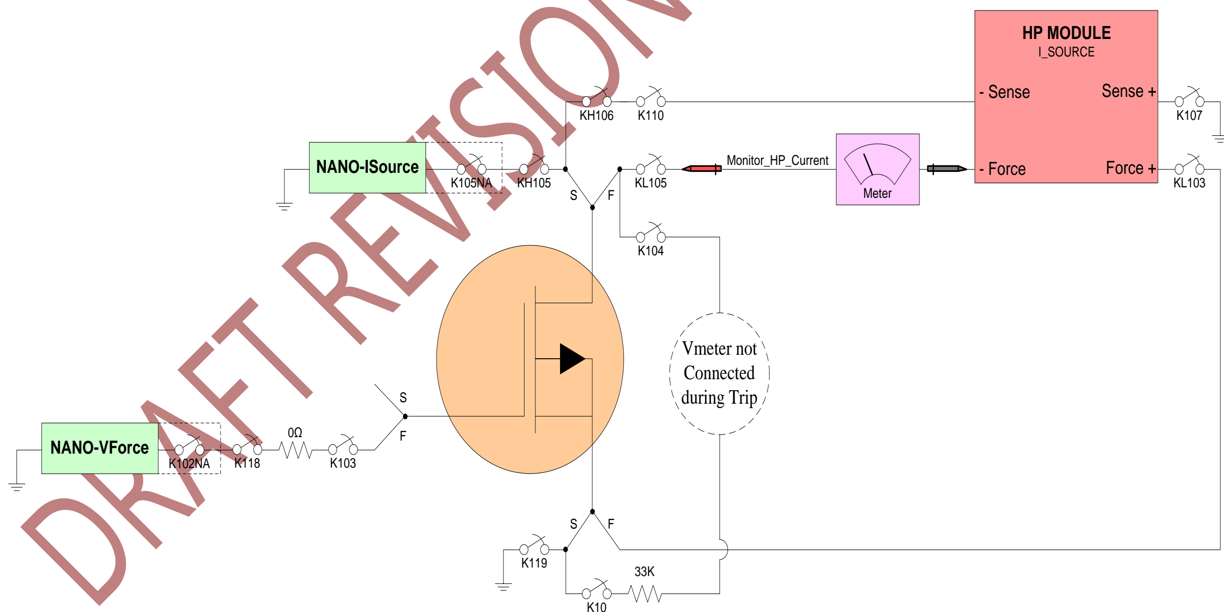
Condition for N-Channel device heating pulse.



Condition for P-Channel device heating pulse.



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TRIP_TSN Test Parameters

TRIP_TSN Configuration

Test Method Configuration

Parameter	Value
Limit	
dTRIP_MAX_OFF	**dTRIP_MAX_OFF**
dTRIP_MAX_ON	**dTRIP_MAX_ON**
dTRIP_MIN_OFF	**dTRIP_MIN_OFF**
dTRIP_MIN_ON	**dTRIP_MIN_ON**
pTRIP_TEMP_MAX	**pTRIP_TEMP_MAX**
pTRIP_TEMP_MIN	**pTRIP_TEMP_MIN**
TRIP_TEMPMAX	**TRIP_TEMPMAX**
TRIP_TEMPMIN	**TRIP_TEMPMIN**
Misc	
DelayAfterTrip	0.002
DelayBeforeMeas	0.001
DiagData	False
ID_threshold	0.75
ProjectedTemp	False
TripTimeout	0.03
VSD_Meas_Curr	0.005
VsdTempData	False
VsdVgate	0
Setup	
ID_max	10
Kfactor	2
Single_Dual_Die	**Single_or_Die_1**
Tadj	0
TempSensorLocation	**CBits2**
TestMethod	**Both**
Tmb	25
VDS	20
VGS	5

dTRIP_MAX_OFF	This parameter is defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. Defines maximum FET OFF time limit (between FET ON states). Logged trip temperature will be negated if FET maximum OFF time is greater than this limit.
dTRIP_MAX_ON	This parameter is defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. Defines maximum FET ON time limit (between FET OFF states). Logged trip temperature will be negated if FET

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	maximum ON time is greater than this limit.
dTRIP_MIN_OFF	This parameter is defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. Defines minimum FET OFF time limit. Logged trip temperature will be negated if FET maximum OFF time is less than this limit.
dTRIP_MIN_ON	This parameter is defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. Defines minimum FET OF time limit. Logged trip temperature will be negated if FET maximum ON time is less than this limit.
pTRIP_TEMP_MAX ***pTRIP_TEMP_MIN***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. Defines projected temperature maximum limit. This limit is used only if *ProjectedTemp* is set to True.
TRIP_TEMPMAX ***TRIP_TEMPMIN***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. Defines the maximum trip temperature limit. It is suggested not to use a value of NaN for the *TRIP_TEMPMIN* limit because a failing trip condition will force a negative logged trip temperature. A negative value would pass the test limits.
DelayAfterTrip	Minimum amount of time to leave VGS and VDS applied after detection of first trip condition. After the specified *DelayAfterTrip* time value has elapsed, VGS and VDS will remain applied until the next DUT trip edge. The reason for this is to maintain a constant trip edge to Vsd measurement time. (Note that if sufficient time is given to the device for trip cycles to thermally

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	stabilize the die temperature, the extra trip cycle will have little effect on die temperature.) The final trip condition will be limited to a maximum of *dTRIP_MAX_OFF* + *dTRIP_MAX_ON*, but will be shorter, dependant on the DUT trip characteristics. A special value of 1.23e-6 is used to enable a fixed heating pulse width (plus additional time as mentioned in previous paragraph). *TripTimeout* is used to define the pulse width.
DelayBeforeMeas	Amount of time, in seconds, between the heating pulse and the final Vsd measurement.
DiagData	Set to True to enable additionally log of FET maximum measured duration ON and OFF times.
ID_threshold	Defines Drain-Source heating pulse current, in amps, for trip condition. A measured ID less than this parameter will be considered a trip (FET OFF) condition.
ProjectedTemp	Set True to compute (or project backwards in time) the final Vsd value to the time of final trip condition. When using the projected temperature method, it is suggested to use a *DelayBeforeMeas* value of 100-200usec. This provides sufficient settling time for the instrument transition from heating pulse to Vsd measurement.
TripTimeout	Maximum time to wait for a trip condition. If the *DelayAfterTrip* value is 1.23e-6, then *TripTimeout* defines the heating pulse width.
VSD_Meas_Curr	Amount of current to apply when measuring initial (ambient) and final Vsd voltage.
VsdTempData	False to disable logging of Vsd and Tmb (or temperature sensor) data. Default is True.
VsdVgate	Can be used to set Gate voltage near expected Drain Vsd

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	voltage. While this is not exactly Gate tied to Drain, it closely approximates the condition and eliminates Gate to Source parasitic issues. Use a negative value for N-Channel devices, as a negative current is applied to the Drain pin for Vsd measurements.
ID_max	Specifies maximum Drain-Source (ID) current allowed to apply during heating pulse. *ID_max* is typically set higher than current conducted by the FET during the heating pulse.
Kfactor	Defines the Kfactor, in mV/°C, used in the temperature computation.
Single_Dual_Die	Used to select which die Vsd ambient measurement is associated with. This parameter has meaning only with an external DualDieMux attached.
Tadj	Trip temperature compensation correction factor.
TempSensorLocation	Defines location of ambient temperature sensor. If **None** is selected, will use the *Tmb* value for the temperature computation. This parameter has meaning only with an external DualDieMux attached.
TestMethod	Provides ability to designate the test as the initial (ambient) Vsd measurement only, trip test only (uses initial ambient Vsd measurement for delta-Vsd calculation), perform both initial ambient and final Vsd after heating pulse. A special condition is provided to measure Vsd only, but not retain the value. This method can be used to measure Vsd of FET at any time during the test flow. If *TestMethod* is set to *Trip_Only* and Vsd has not been

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	previously measured, the TRIP_TSN test will perform an initial ambient measurement anyway.
Tmb	If an external temperature sensor is not used, *Tmb* allows entry of an estimated or externally measured ambient temperature.
VDS	Defines amount of Drain-Source voltage to apply during the heating pulse.
VGS	Defines amount of Gate-Source voltage to apply during the heating pulse.

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TRIP_TSN_Loop Test

Overview:

Quickly measure specifically designed FET trip temperature several times within the test.

Description:

Since this test logs a temperature, it is suggested to measure Vsd (intrinsic diode voltage) prior to parametric testing while the die is still at ambient temperature. This value is then saved and used as part of the trip temperature that occurs latter in the test flow.

Vsd is measured by placing a small current through the intrinsic diode and measuring the voltage across the diode. The Vsd Measurement Schematic shows the method for Vsd measurement.

The ambient Vsd is measured prior to heating the die. The final Vsd is measured after the die has been heated.

To heat the die, apply *VGS* (Gate voltage) and *VDS* (Drain-Source voltage) voltages. (Refer to the heating schematics below.) The trip test will wait for the first trip condition (ID current less than *ID_Threshold*), or for maximum of *TripTimeout*.

If the FET did not achieve trip condition within the *TripTimeout*, the logged trip temperature will be negated.

If the *DelayAfterTrip* value is greater than 0, the test will continue to apply VGS and VDS for the *DelayAfterTrip* time (plus time for the FET to achieve final trip condition). During this time, the test will monitor the duration of FET ON and OFF times and retain the largest ON and OFF time detected.

If the detected ON time is greater than *dTRIP_MAX_ON* or less than *dTRIP_MIN_ON*, the logged trip temperature will be negated, if not already a negative value.

If the detected OFF time is greater than *dTRIP_MAX_OFF* or less than *dTRIP_MIN_OFF*, the logged trip temperature will be negated, if not already a negative value.

The trip temperature is computed by the following formula:

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Ttrip (°C) = (ABS(Vsd_final – Vsd_ambient) / (*Kfactor* / 1000)) + *Tmb* + *Tadj*.

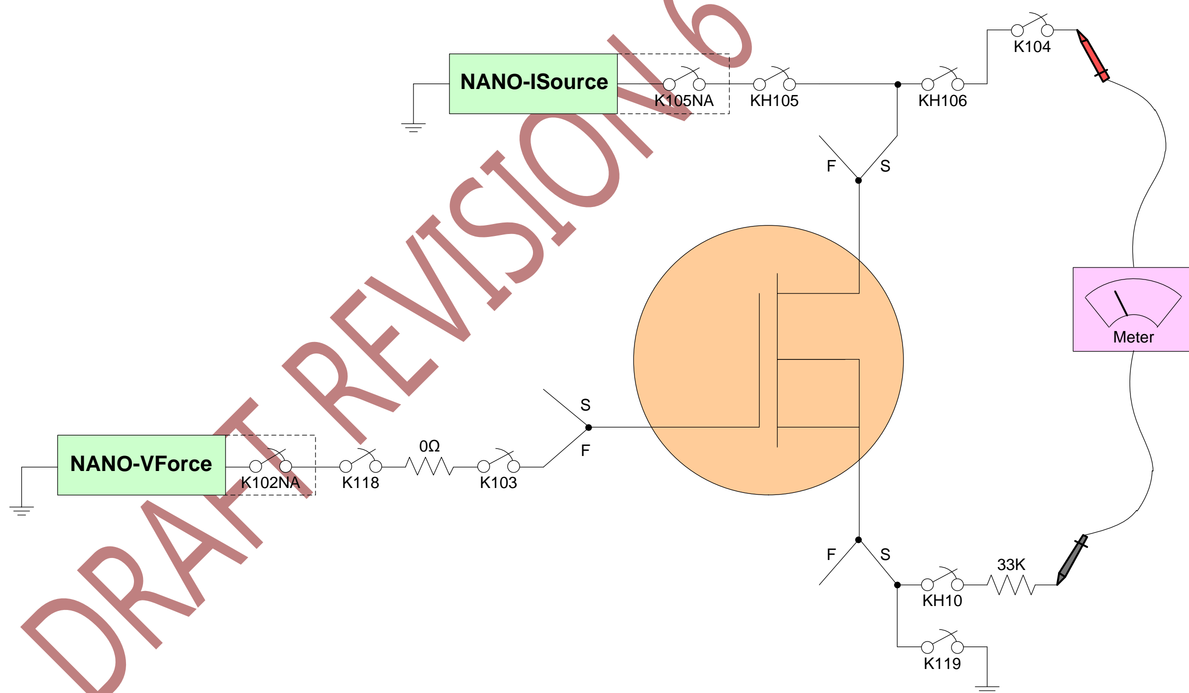
There is a special mode that can produce a *VGS* & *VDS* voltage for a fixed period of time (plus time for FET to achieve final trip condition), no matter when the FET trips. This is accomplished by setting the *DelayAfterTrip* value to exactly 1.23e-6 and setting the *TripTimeout* to the desired pulse width.

During the fixed trip pulse width mode, the test will detect the longest duration of FET ON and OFF times (following first time trip). These times will be tested against the respective limits (as mentioned above).

If the FET did not trip during the fixed pulse width, the temperature will be negated.

TRIP_TSN_Loop Test Schematics

Condition for measuring Vsd of N-Channel or P-channel devices.



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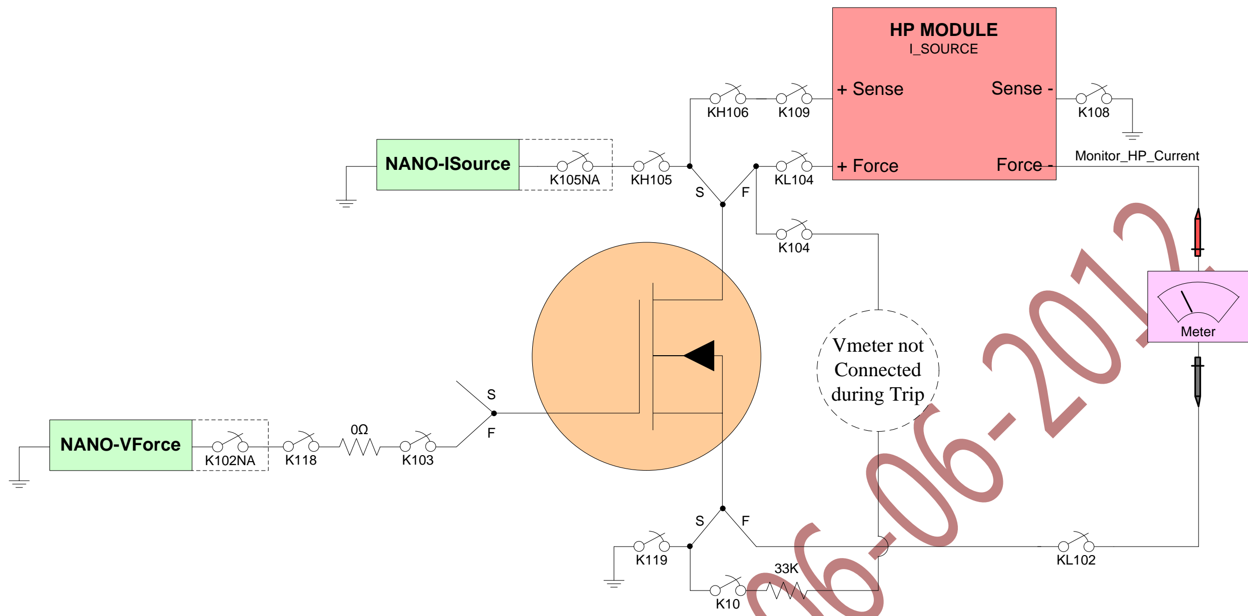
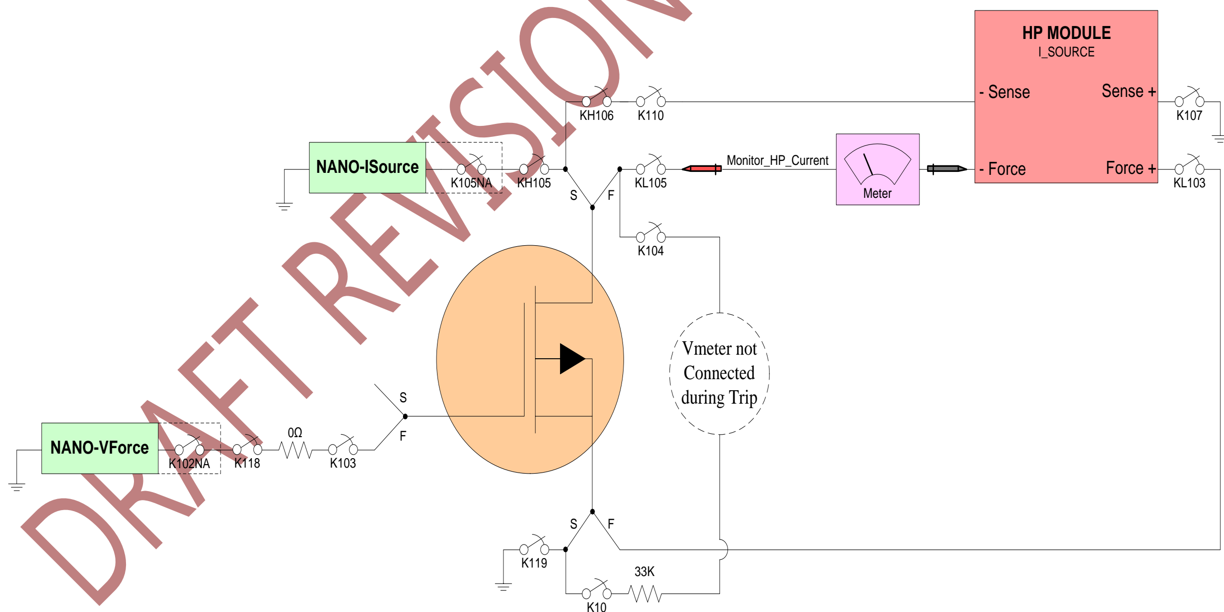
Condition for N-Channel device heating pulse.



Condition for P-Channel device heating pulse.



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TRIP_TSN_Loop Test Parameters

TRIP_TSN_Loop Configuration

Test Method Configuration

Parameter	Value
Limit	
TRIP_MAXTIME	**TRIP_MAXTIME**
TRIP_MINTIME	**TRIP_MINTIME**
TRIP_TEMPMAX	**TRIP_TEMPMAX**
TRIP_TEMPMIN	**TRIP_TEMPMIN**
Misc	
DataPerLoop	False
DelayBeforeMeas	0.0005
PreheatPulseWidth	0
PreheatStabilize	0.01
VSD_Meas_Curr	0.005
Setup	
DualDieMUX	**None**
Kfactor	2.2
Single_Dual_Die	**Single_or_Die_1**
Tadj	0
TestMethod	**Both**
Tmb	25
TripLoops	1
VDS	20
VGS	5

Parameter	Description
TRIP_MAXTIME ***TRIP_MINTIME***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. Defines maximum and minimum time for FET to achieve trip state.
TRIP_TEMPMAX ***TRIP_TEMPMIN***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. Defines trip temperature limits.
DataPerLoop	Set True to additionally log trip temperature for each loop iteration. False will log only final loop iteration trip temperature result.

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DelayBeforeMeas	Amount of time between the heating pulse and the Vsd measurement.
PreheatPulseWidth	Amount of time to apply VDS and VGS prior to temperature trip detection.
PreheatStabilize	Amount of FET off time between *PreheatPulseWidth* and temperature trip detection heating pulse test phases.
VSD_Meas_Curr	Amount of current to apply when measuring Vsd voltages.
DualDieMux	Defines location of ambient temperature sensor. If **None** is selected, will use the *Tmb* value for the temperature computation. This parameter is used only if an external DualDieMux is attached.
Kfactor	Defines the Kfactor, in mV/°C, used in the temperature computation.
Single_Dual_Die	Used to select which die Vsd ambient measurement is associated with. This parameter is used only if an external DualDieMux is attached.
Tadj	Trip temperature compensation correction factor.
TestMethod	Provides ability to designate the test as the initial (ambient) Vsd measurement only, trip test only (uses initial ambient Vsd measurement for delta-Vsd calculation), or perform both initial ambient and final Vsd after heating pulse. If *TestMethod* is set to *Trip_Only* and Vsd has not been previously measured, the TRIP_TSN test will perform an initial ambient measurement anyway.
Tmb	If an external temperature sensor is not used, *Tmb* allows entry of an estimated or externally measured ambient temperature.

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TripLoops	Specifies the quantity of temperature trip events to perform.
VDS	Defines amount of Drain-Source voltage to apply during the heating pulse.
VGS	Defines amount of Gate-Source voltage to apply during the heating pulse.

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V_Status Test

Overview:

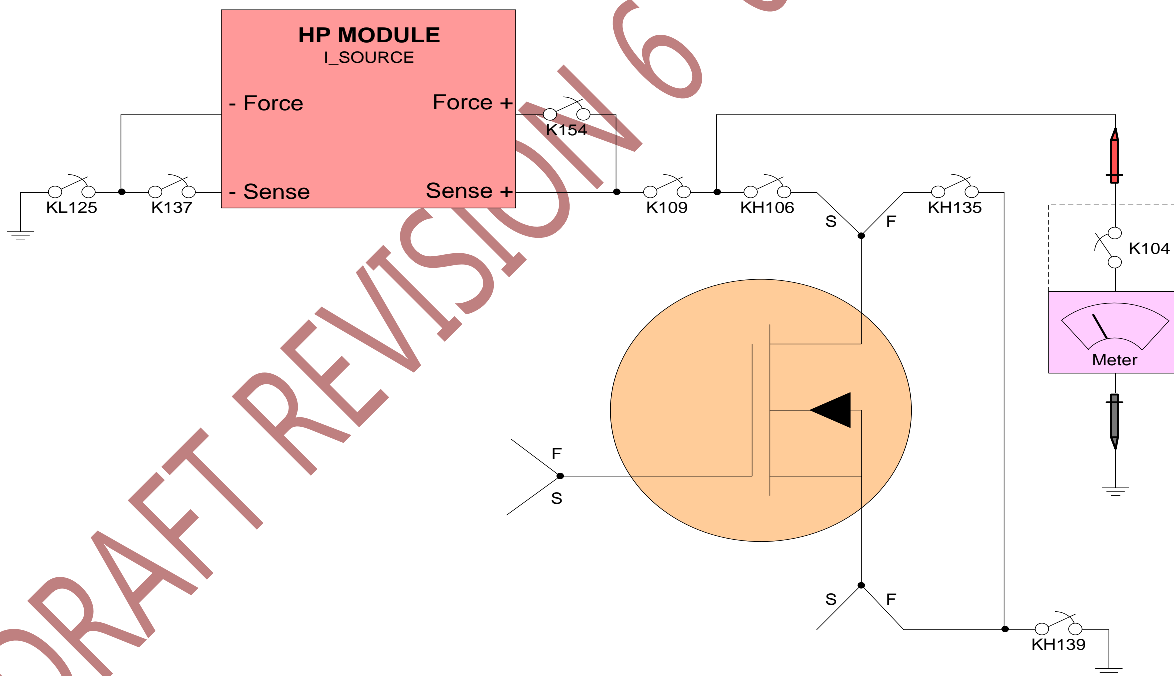
Test Drain-Sense to Drain-Force socket, handler, or prober contact integrity.

Description:

Apply 100mA (limited to 10V) to Drain-Sense pin. Drain-Force is connected to Source-Force and Ground. Measure voltage from Drain-Sense to Ground. If the voltage is greater than 194mV, the test fails.

V_Status Test Schematic

Condition for N-Channel or P-Channel devices.



V_Status Test Parameters

There are no parameters for this test.

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VDSON Test

Overview:

Measure Drain-Source voltage with MOSFET turned on.

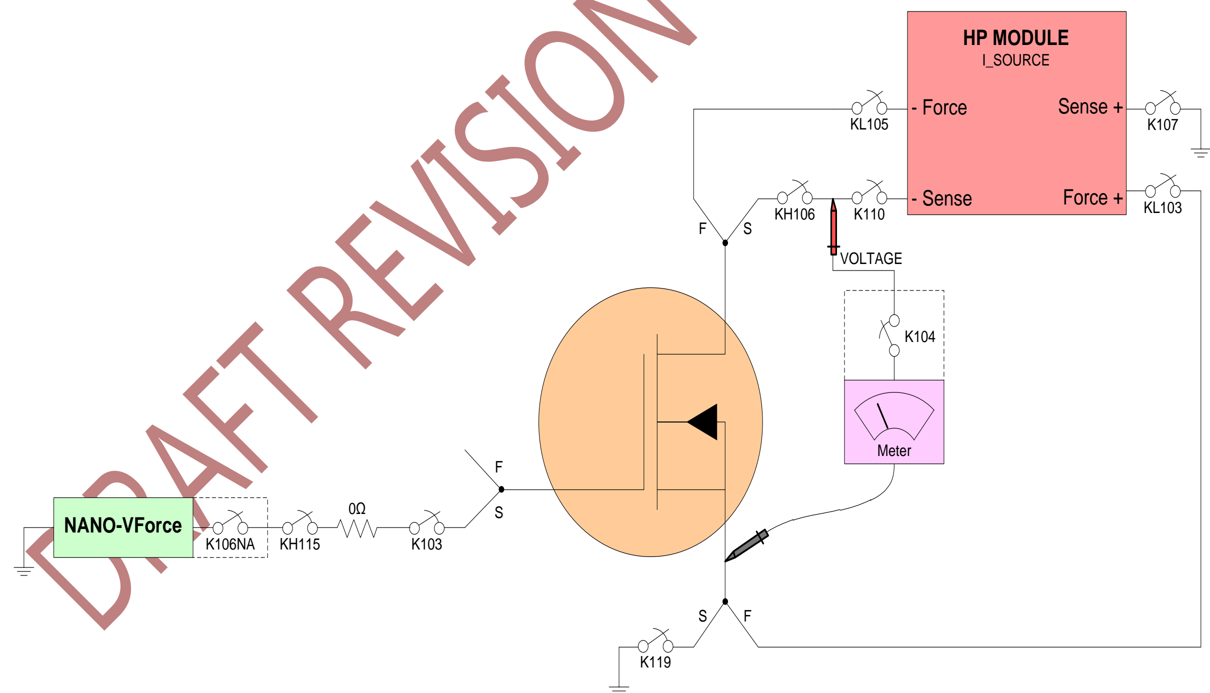
For ID currents less than 25mA, use the VDSON_LV test instead. It will produce more accurate results.

Description:

Turn the FET on with VGS Gate voltage. Apply Drain-Source current of ID amps and measure the voltage across the Drain-Source.

VDSON Test Schematics

Condition for N-Channel device.



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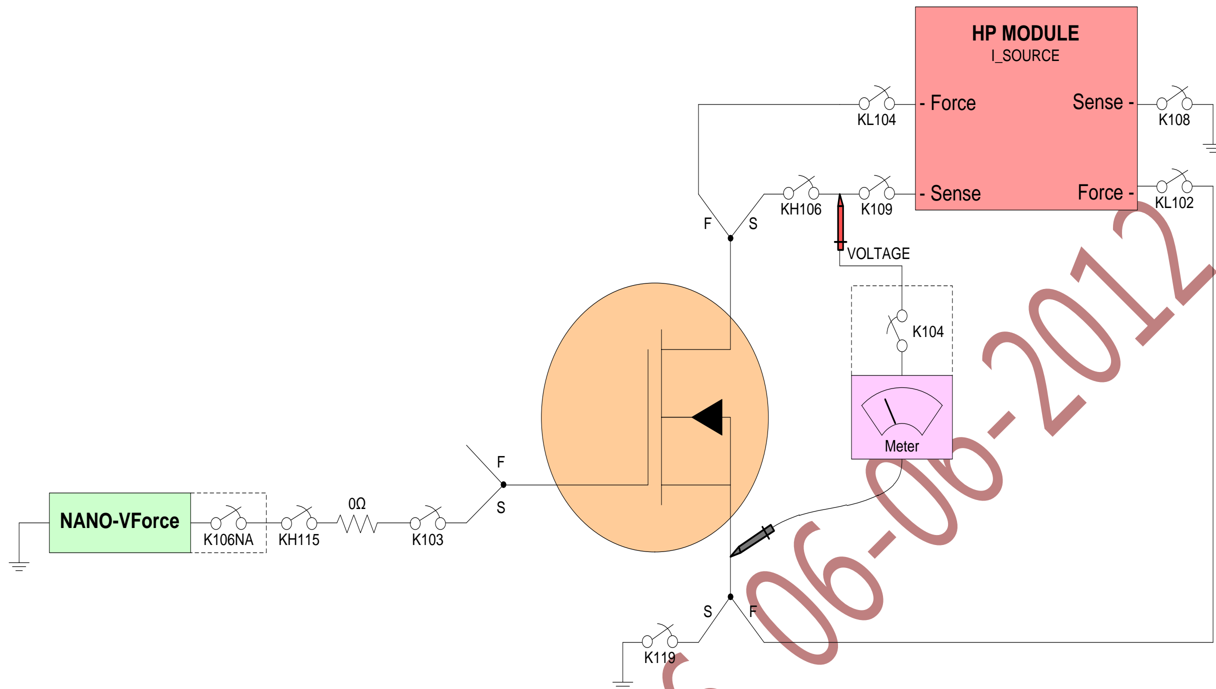
Condition for P-Channel device.



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VDSON Test Parameters

VDSON Configuration

Test Method Configuration

Limits	
VDSON_Max	**VDSON_Max**
VDSON_Min	**VDSON_Min**
Misc	
CalSettlingTime	0.0005
Compensation	**MediumSlow**
DebugData	False
EngMode	False
IDSettlingTime	0.0005
Samples	10
Setup	
ID	10
VGS	10

VDSON_Max ***VDSON_Min***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. These values are dependent upon device

	specification.
CalSettlingTime	Not used. Value will be ignored.
Compensation	Used to adjust ID supply performance. If a device oscillates during the test pulse, changing this value so some other compensation setting may eliminate the oscillation.
DebugData	Not used. Setting will be ignored.
EngMode	Not used. Setting will be ignored.
IDSettlingTime	This is actually the test pulse width, in seconds. This is variable depending on the component(s) being tested. Adjust the pulse (typical increase) until a stable reading is achieved.
Samples	Number of samples to average for measurement result Sample rate is 11.6usec per sample. If the quantity of *Samples* is increased, it may be necessary to increase *IDSettlingTime* as well.
ID	Amount if Drain-Source current to apply, in amps.
VGS	Gate voltage to apply during the test pulse.

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VDSON25mAmax Test

Overview:

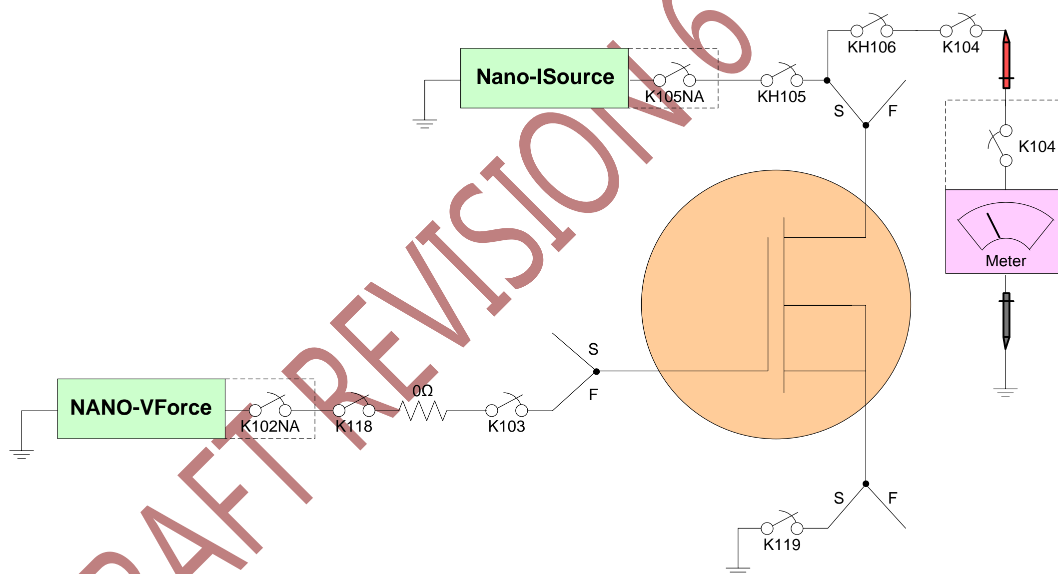
This test operates the same as the *VDSON* test but uses a lower power supply of 25 milliamp max.

Description:

Turn the FET on with VGS Gate voltage. Apply Drain-Source current of ID amps and measure the voltage across the Drain-Source.

VDSON25mAmax Test Schematic

Configuration for N-Channel or P-Channel devices.



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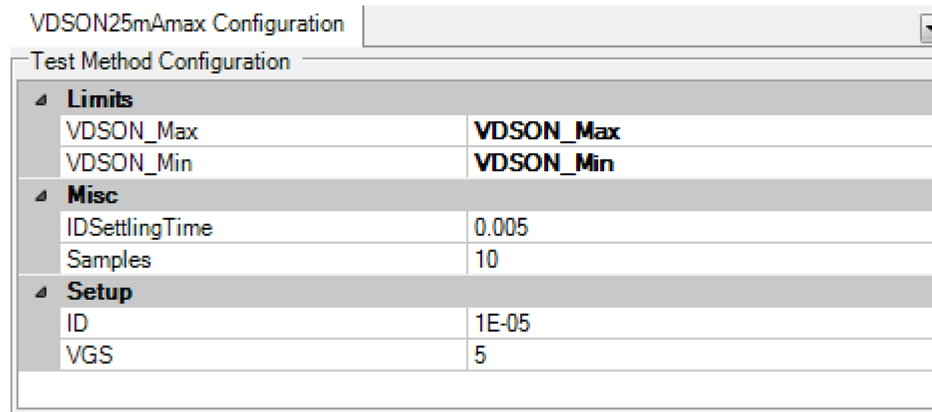
VDSON25mAmax Test Parameters



VDSON_Max ***VDSON_Min***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. These values are dependent upon device specification.
IDSettlingTIme:	This is actually the test pulse width, in seconds. This is variable depending on the component(s) being tested. Adjust the pulse (typically increase) until a stable reading is achieved.
Samples:	Number of samples to average for measurement result. Sample rate is 11.6usec per sample. If the quantity of *Samples* is increased, it may be necessary to increase *IDSettlingTime* as well.
ID:	Amount if Drain-Source current to apply, in amps.
VGS:	Gate voltage to apply during the test pulse.

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VGD Test

Overview:

Typically used to measure test circuit resistor between Drain-Sense and Gate-Force DUT fixture connection.

Description:

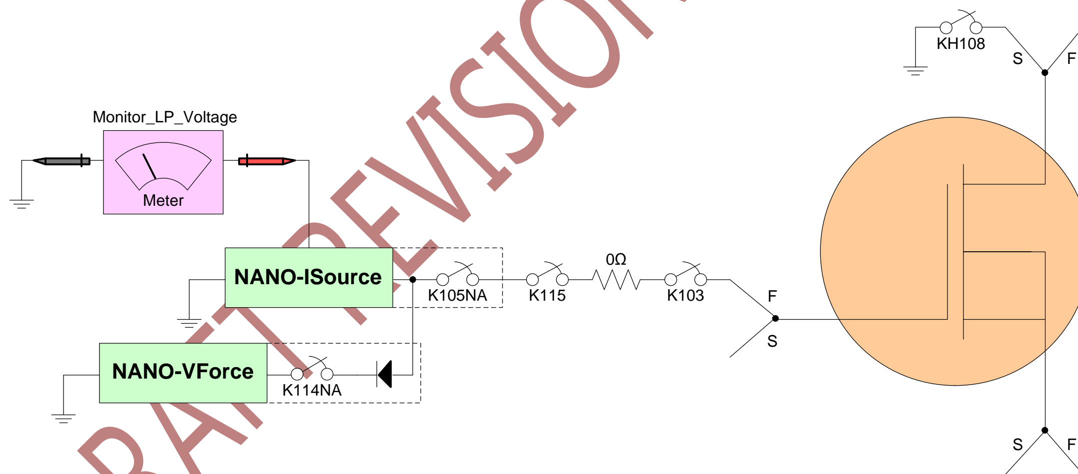
Apply *ID* current (current source limited to 10V) to Gate-Force tester port. Current return path is from Drain-Sense tester port to Ground. Measure and report voltage at the Gate-Force port.

If measuring resistor, resistance can be computed by:

R = V (logged result) / I (*ID*).

VGD Test Schematics

Condition for N-Channel device or positive *ID* current specified.



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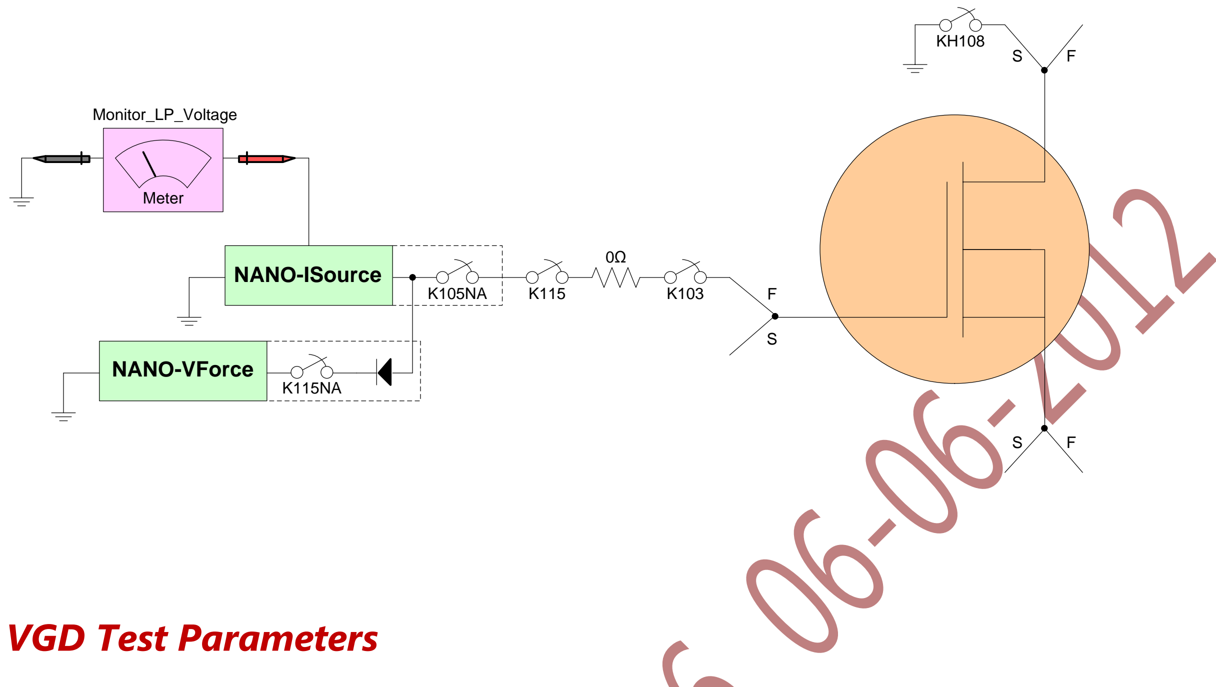
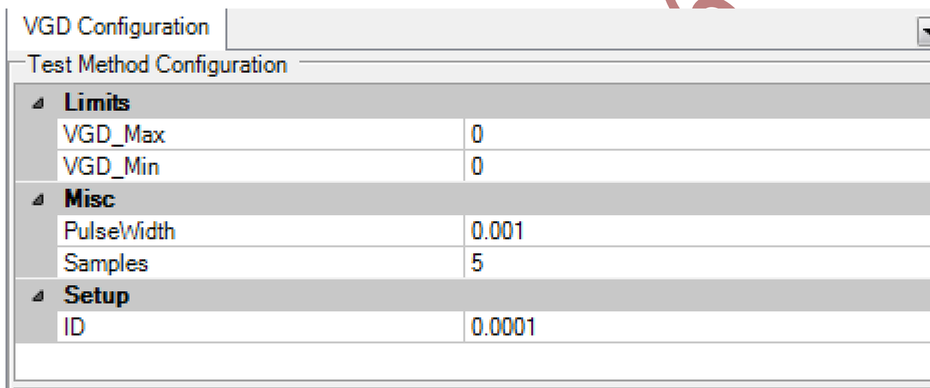
Condition for P-Channel device or negative *ID* current specified.



VGD Test Parameters



VGD_Max ***VGD_Min***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. These define the Gate-to-Drain voltage limits.
PulseWidth	Length of time, in seconds, to apply each voltage pulse. This is variable depending on the component(s) being tested. Adjust the pulse (typically increase) until a stable reading

	is achieved.
Samples	Number of measurement samples to average for result. Sample rate is 11.6usec per sample. If quantity of *Samples* is increased, may need to increase *PulseWidth* accordingly.
ID	Amount of current to apply. Current source supply voltage output is limited to 10 volts.

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VGS Test

Overview:

Measure Gate voltage required to achieve a specific ID.

The VGS test is limited to +/-25V.

Description:

Apply ID current to Drain and Gate (which sees only the voltage component) then measure and log Gate-Source voltage.

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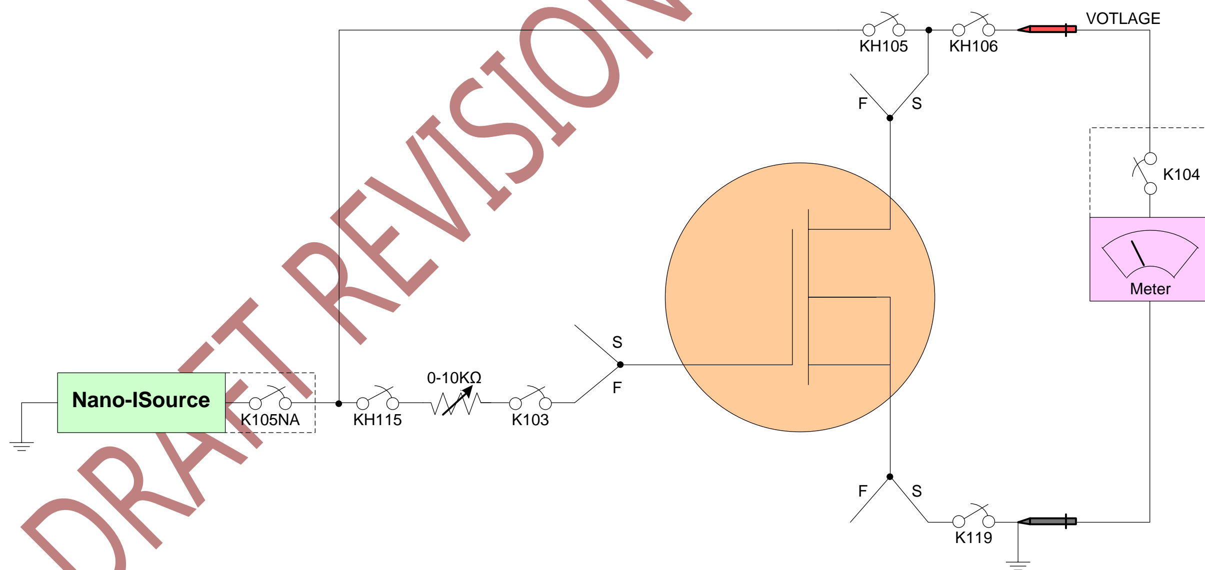
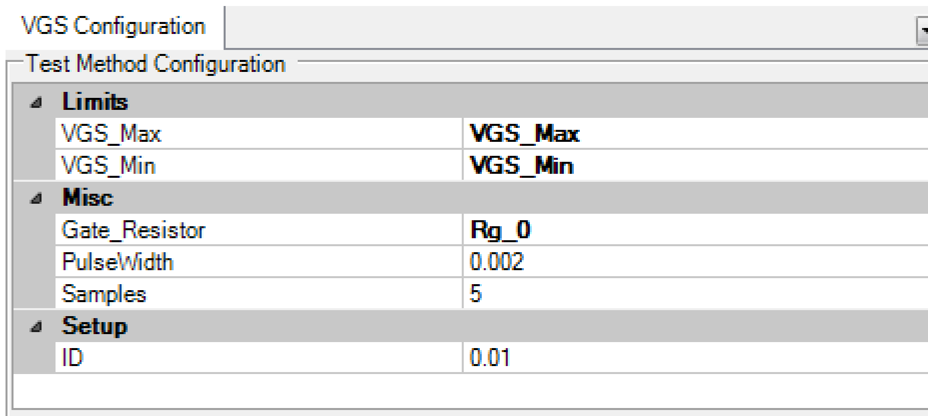
VGS Test Schematics

Condition for N-Channel of P-Channel devices.



VGS Test Parameters



VGS_Max **VGS_Min**	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. These values are dependent upon device specification.
Gate_Resistor	Dependent upon device to prevent oscillation. If device oscillates, try different resistor values. Note: Actual resistance may not be represented by the selection text.
PulseWidth	Length of time, in seconds, to apply each voltage pulse. This is variable depending on the component(s) being tested. Adjust the pulse (typically increase) until a stable reading is achieved.
Samples	Number of samples to average for measurement result. Sample rate is 11.6usec per sample.
ID	Amount of current, in amps, to apply during the test pulse.

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VSD Test

Overview:

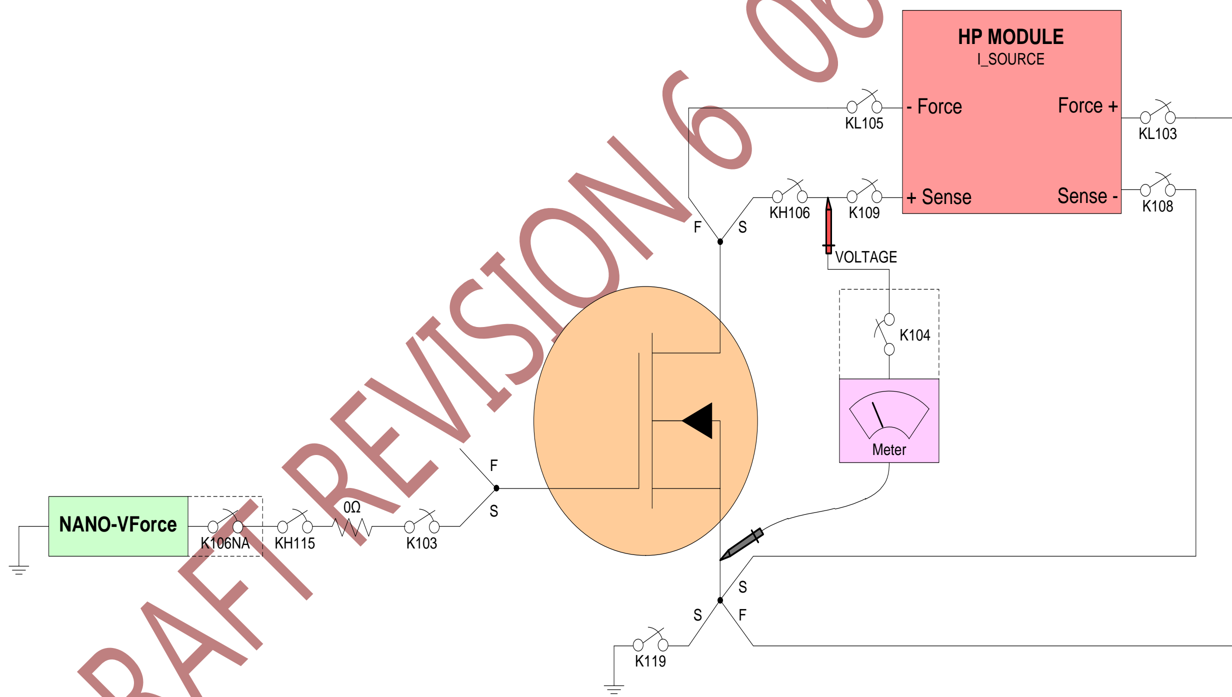
Measure the voltage drop across the FET intrinsic diode (Source-Drain).

Description:

Apply *IS* current from Source to Drain, measure and log voltage across Source-Drain.

VSD Test Schematics

Condition for N-Channel device.



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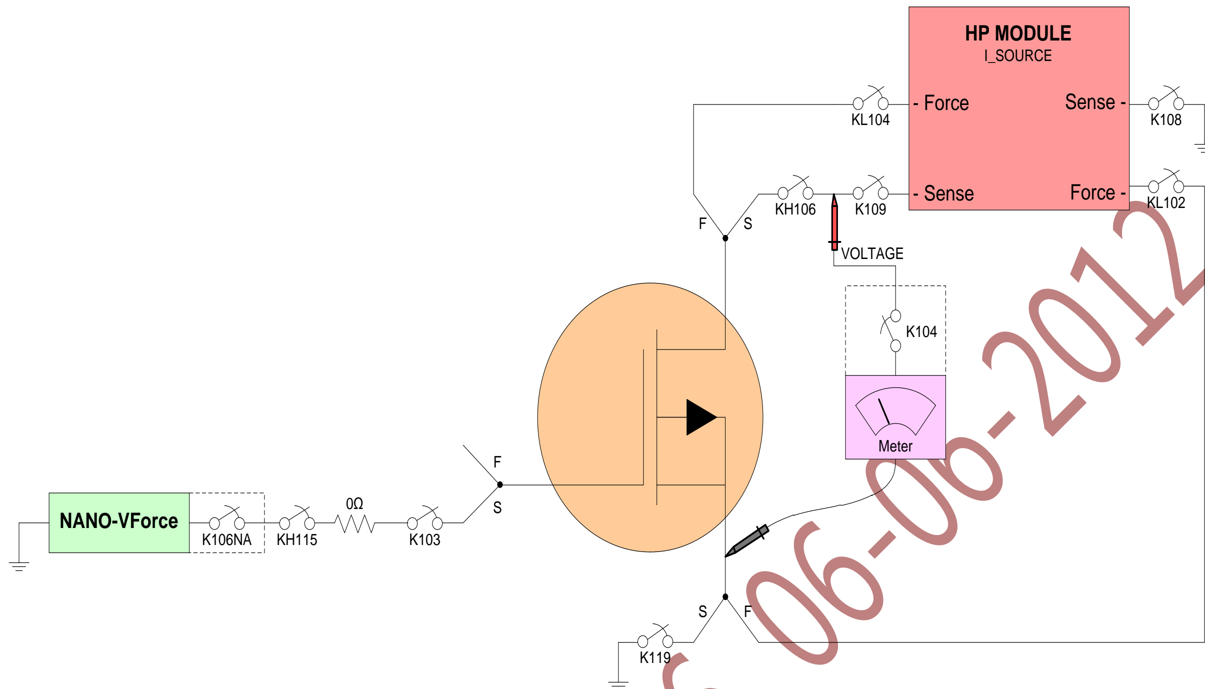
Condition for P-Channel device.



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VSD Test Parameters

VSD Configuration

Test Method Configuration

Limits	
VSD_Max	**VSD_Max**
VSD_Min	**VSD_Min**
Misc	
Compensation	**MediumSlow**
PulseWidth	0.0003
Samples	5
Setup	
IS	1
VGS	0

VSD_Max ***VSD_Min***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields.

	These values are dependent upon device specifications.
Compensation	Used to adjust ID supply performance. If a device oscillates during the test pulse, changing this value so some other compensation setting may eliminate the oscillation.
PulseWidth	Length of time, in seconds, to apply each voltage pulse. This is variable depending on the component(s) being tested. Adjust the pulse (typically increase) until a stable reading is achieved.
Samples	Number of samples to average for measurement result. Sample rate is 11.6usec per sample. If the quantity of *Samples* is increased, it may be necessary to increase the *PulseWidth* accordingly.
IS	Source-to-Drain current, in amps, to apply.
VGS	Gate voltage to apply during test.

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VTH Test

Overview:

Determine amount of Gate voltage required to achieve a specific ID at a given VDS.

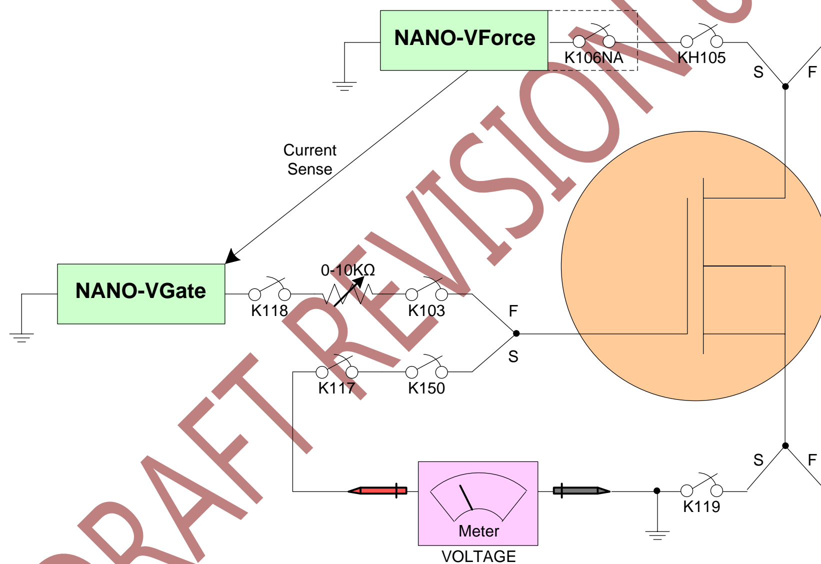
> The VTH test is limited to +/-25V and +/- 100mA. If test conditions greater than this are required, must use the VTH_Digi test.

Description:

Apply *VDS* voltage to Drain-Source and adjust Gate voltage until desired *ID* is achieved. Measure and log Gate voltage.

VTH Test Schematics

Condition for N-Channel or P-Channel devices.



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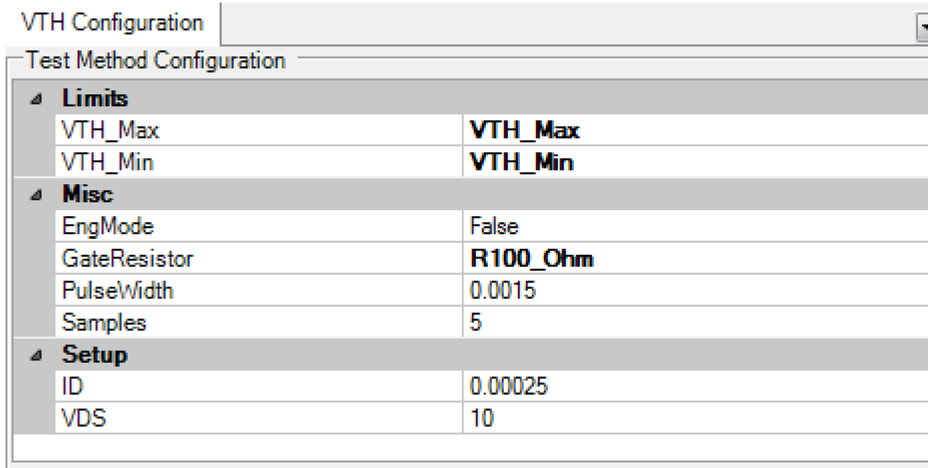
VTH Test Parameters



VTH_Max ***VTH_Min***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. These values are dependent upon device specification.
EngMode	True to add include applied current in the logged description field.
GateResistor	Dependent upon device to prevent oscillation. If device oscillates, try different resistor values.
PulseWidth	Length of time, in seconds, to apply each voltage pulse. This is variable depending on the component(s) being tested. Adjust the pulse (typically increase) until a stable reading is achieved.
Samples	Number of measurement samples to average. Sample rate is 11.6usec per sample. If quantity of *Samples* is increased, it may be necessary

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	to increase *PulseWidth* accordingly.
ID	Amount of Drain-Source current, in amps, to achieve. *ID* is limited to +/-100mA.
VDS	Amount of Drain-Source voltage to apply. *VDS* is limited to +/-25V.

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VTH_Digi Test

Overview:

This is the same type of test as VTH except in a digitized format. This test allows for more current and voltage than the VTH test; 100 amps currently. Additionally *VTH_Digi* does not require the hardware to stabilize the loop at a given current

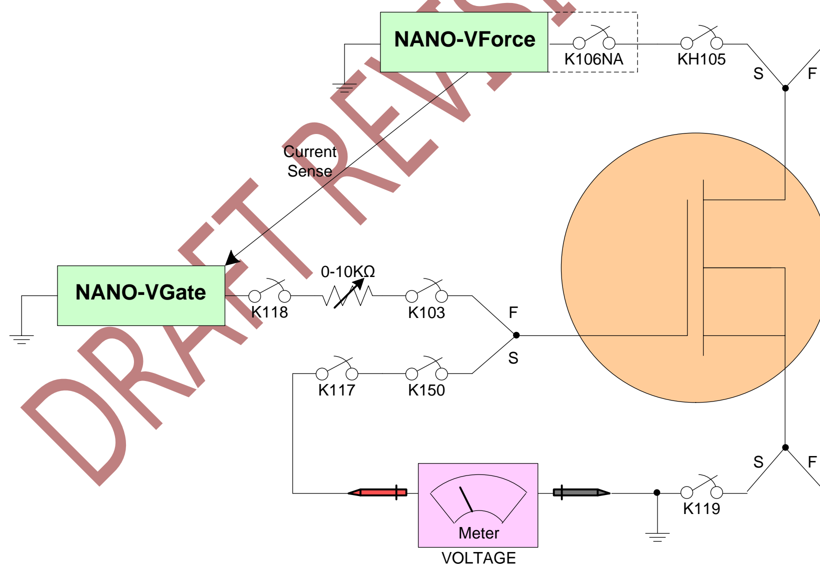
Description:

Apply VDS voltage to the Drain-Source. Set the Gate to the *VgsStart* voltage and increment the Gate voltage at a rate of *VgsStep* until either *VgsMax* is achieved, or the greater of ID1 or ID2 is achieved.

The Gate voltage is then decremented by *VgsStep* until *VgsStart* is achieved, or ID reduces to less than *ID1* (if *ID1* is not 0) or *ID2* is achieved.

VTH_Digi Test Schematics

For *VDS* voltages less than or equal to +/-25V and currents less than 100mA, test will use the following configuration for both N-Channel or P-Channel devices.



Unlike the *VTH* test, the *VTH_Digi* test will ramp the NANO-VGate supply until the desired *ID* is achieved, as reported by the NANO-VForce instrument.

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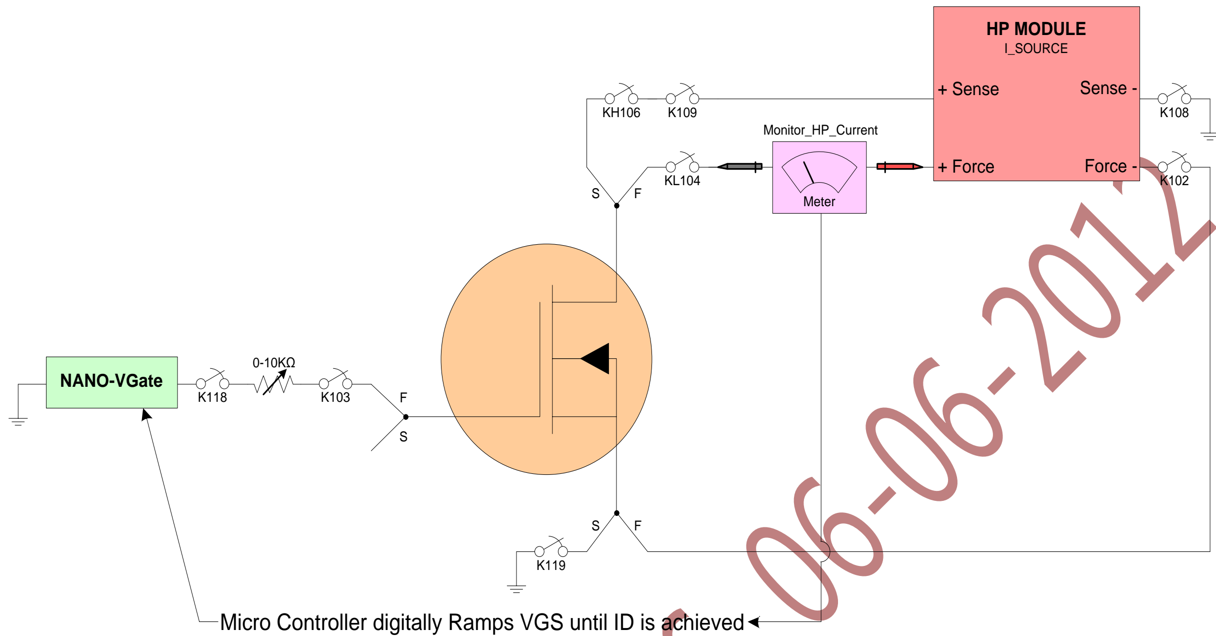
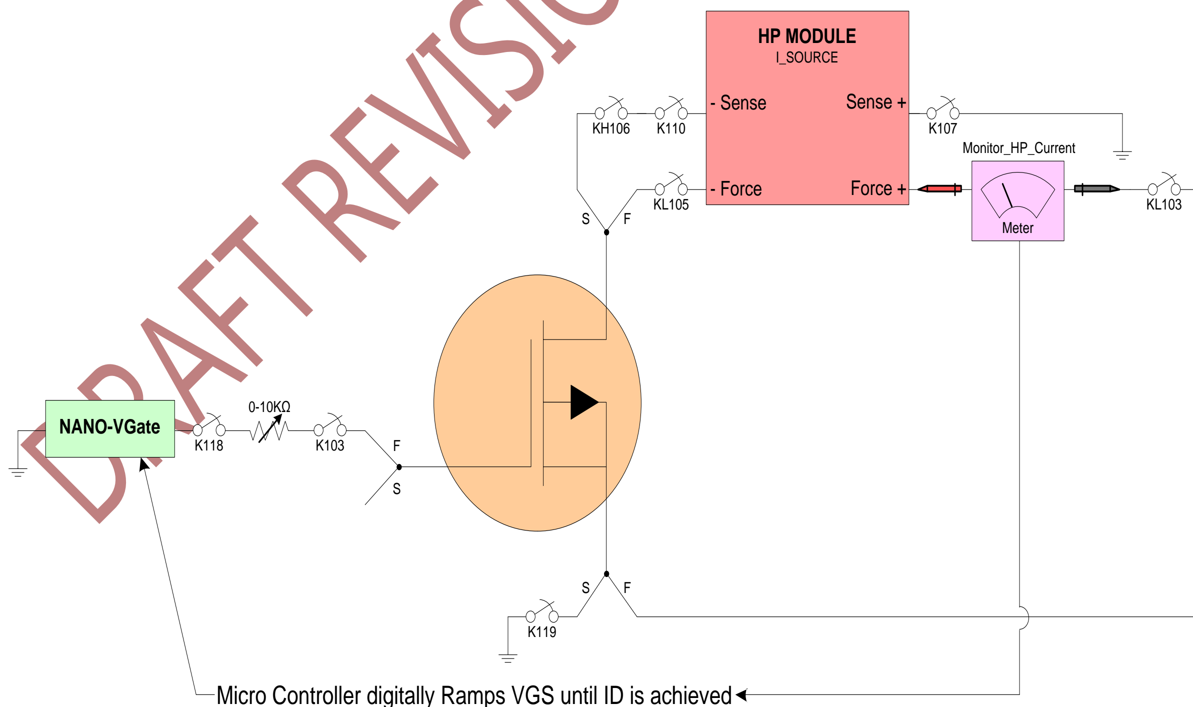
For *VDS* voltages up to 55V and ID currents greater than 100mA, the *VTH_Digi* test will use the following configuration for N-Channel devices.



For *VDS* voltages up to 55V and ID currents greater than 100mA, the *VTH_Digi* test will use the following configuration for P-Channel devices.



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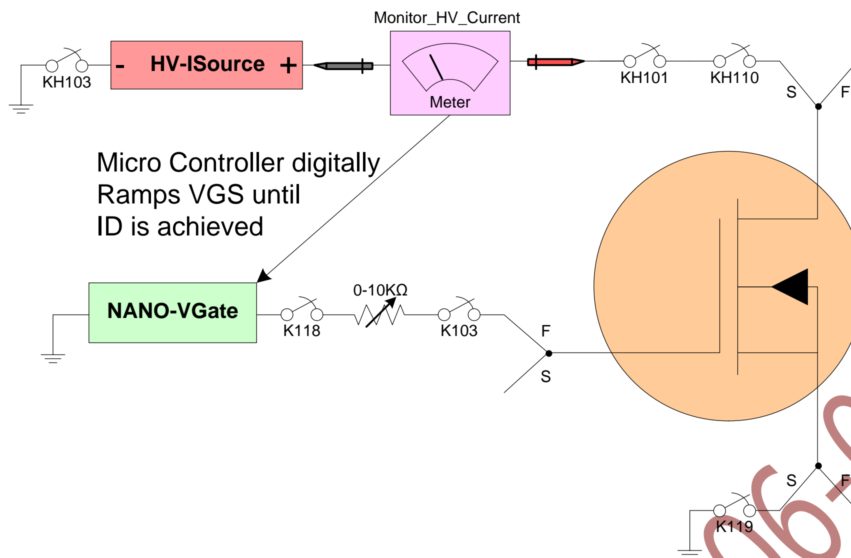
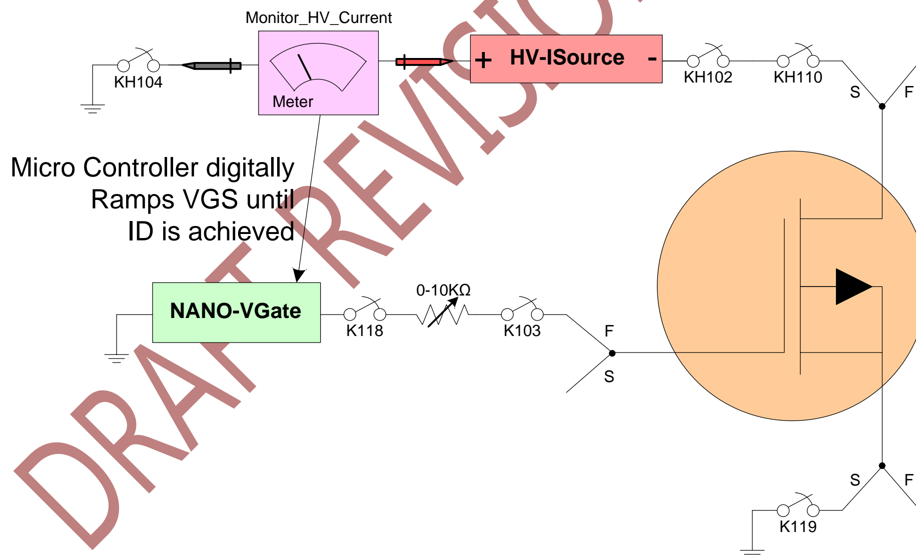
For *VDS* voltages above 25V and ID currents less than 100mA, the *VTH_Digi* test will use the following configuration for N-Channel devices.



For *VDS* voltages above 25V and ID currents less than 100mA, the *VTH_Digi* test will use the following configuration for P-Channel devices.



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VTH_Digi Test Parameters

VTH_Digi Configuration

Test Method Configuration

Limits	
VTH1_Max	**VTH1_Max**
VTH1_Min	**VTH1_Min**
VTH2_Max	**VTH2_Max**
VTH2_Min	**VTH2_Min**
Misc	
DebugData	**Off**
GateResistor	**R100_Ohm**
VgsMax	8
VgsStart	1
VgsStep	0.01
Setup	
ID1	0
ID2	5
VDS	10
Z_Power_User	
ForceHv	False

VTH1_Max ***VTH1_Min***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. These values are dependent upon device specification. These limits are associated with *ID1* setup parameter condition.
VTH2_Max ***VTH2_Min***	These parameters are defined on the *Program Variables* tab or can be changed by directly typing the values in the fields. These values are dependent upon device specification. These limits are associated with *ID2* setup parameter condition.
DebugData	Ability to enable additional data logging. **Off** – No debug data will be logged.

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	PulseWidth – Log effective VTH measurement pulse width. The pulse width is computed for the duration that ID is greater than 30% of the larger of *ID1* or *ID2* setup parameters. **Display_Measured_Vgs_and_Ids_Points** – Log measurement pulse width, measured Ids on each side of *ID1* setup parameter, and measured Ids on each side of *ID2* setup parameter. **Display_All_Measured_Points** – Log up to the first 200 Vgs forcing and Ids measurement value pairs taken during the ramping operation.
GateResistor	Dependent upon device to prevent oscillation. If device oscillates, try different resistor values.
VgsMax	Defines maximum Vgs voltage allowed to apply if target *ID1* or *ID2* is not achieved. To minimize test time if target ID is not achieved, limit this value to a realistic FET Vgs full turn on condition.
VgsStart	Defines the Vgs voltage to apply at the beginning of the ramping operation. To minimize test time, set this to a value that would be close to the FET Gate turn-on voltage, but low enough that the FET does not conduct current.
VgsStep	Defines the resolution to step the Gate voltage during the VTH ramp operation. If this value is too small, will increase test time and also overheat the DUT. If this value is too large, will cause large Ids current steps. Suggest start with large *VgsStep* value on samples with

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	lower ID setting to determine desired Ids step results.
ID1	Can be used to measure and log a second VTH result, typically at a lower ID current than *ID2*. Enter a value of 0 to disable logging of this second condition. The *VTH1_Max* and *VTH1_Min* limits are associated with this setup parameter.
ID2	Defines ID current to achieve for VTH result. This value cannot be 0. The *VTH2_Max* and *VTH2_Min* limits are associated with this setup parameter.
VDS	Defines Drain-Source voltage to apply for VTH test.
ForceHV	True to force use of high voltage supply. False will automatically select best VDS supply to use. On occasion when the ID and VDS parameters are near the supply boundary conditions, it may be desired to force the HV supply usage. The HV supply can deliver a maximum of 100mA and has a useful voltage range of 40-1200V. The HP supply can deliver a useful current range of 20mA to 100A (or 200A depending on HP version installed) and a voltage range up to 55V.

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Chapter 2:
Working with Generic Diagnostic Library Tests

Working with Diagnostic Library6 Tests

- ✓ CBitChecker
- ✓ CommunicationCheck
- ✓ DDM_CC
- ✓ MoboCheck
- ✓ ReadCalResistors

Important Note:

Although the FTI 1000 system you purchased has the ability to run all the tests we provide, some of the tests are specific to the type of equipment you are using including any add on equipment. If your Focused Test representative has not covered or gone over with you specific tests that are to be run on your system(s), any excluded tests are not meant to be run and may result in run time errors..

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CBitChecker Test

Overview:

Test functionality of C-Bit control circuitry.

Description:

Write and read a walking 1 pattern, and a walking 0 pattern through the lower 16 C-Bit controls.

Because the upper 8 bits do not have read-back capability, it is not possible to test those bits with this test.

DC Boards have two (2) C-Bit ports. This test will check both ports.

NOTE: This test may not catch marginal C-Bit control problems.

WARNING: It may be possible to damage some externally connected devices connected to the C-Bits port. It is strongly suggested to remove external hardware connected to the C-Bit ports. (The calibration board is known to be safe to be left connected to the C-Bit port.)

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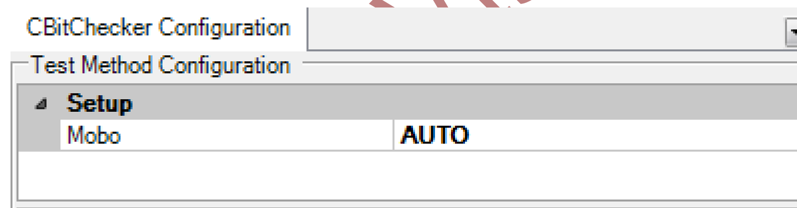
CBitChecker Test Parameters



Mobo	Selects the board for the test. If there is only one board connected to the PC via the USB interface, the selection may be left to the default of Auto.

CommunicationCheck Test

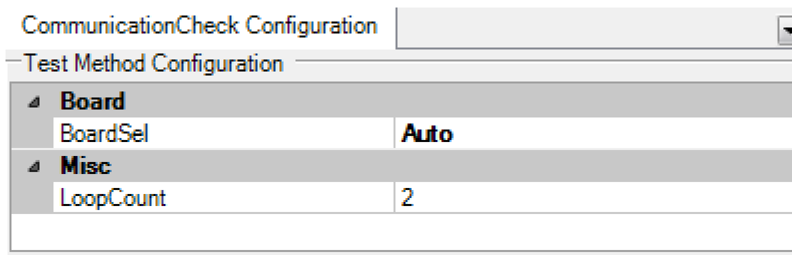
Overview:

Test PC USB to tester integrity.

Description:

Send various commands and patterns to the board and receive expected data in order to test the USB integrity between the PC and tester.

CommunicationCheck Test Parameters



BoardSel	Selects the board for the test. If there is only one board connected to the PC via the USB interface, the selection may be left to the default of Auto.
LoopCount	Defines quantity of test iterations to perform per test run.

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DDM_CC Test

Overview:

Test DualDieMux relays, cabling, and connectors.

Description:

Check that the DualDieMux relays open and close properly, and that there is no cabling/connector open or short.

NOTE: This test requires a special test cable (diagram below) to connect between the DualDieMux DUT connector and a tester spare DB37-pin C-Bits port. (A single tester with an AC only board cannot perform this test. That tester configuration does not have more than one C-Bit port.)

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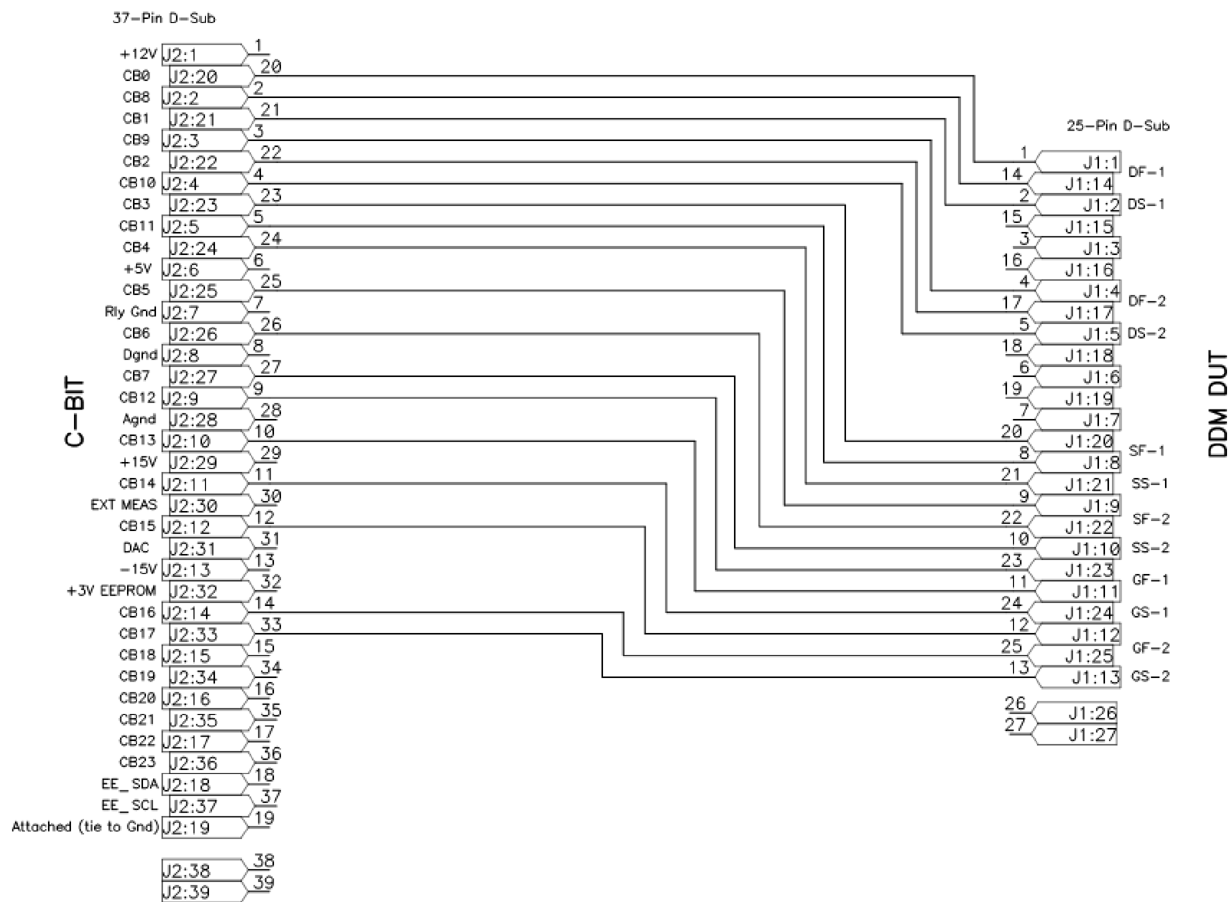

DDM_CC Test Parameters

DDM_CC Configuration

Test Method Configuration

Setup	
CB_DUT	DC_CBits_2
DDM_Ctrl	DC

CB_DUT	Selects the board and C-Bit port that the DualDieMux DUT connector through the special cable is connected to.
DDM_Ctrl	Selects which board that controls the DualDieMux.

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MoboCheck Test

Overview:

Test motherboard FPGA integrity.

Description:

Check various FPGA memories by writing and verifying checker-board and inverse checker-board patterns. Also tests all of the ALU instructions and registers.

Will also perform a shorter version of the *CommunicationCheck* test in order to test the PC to Tester USB interface.

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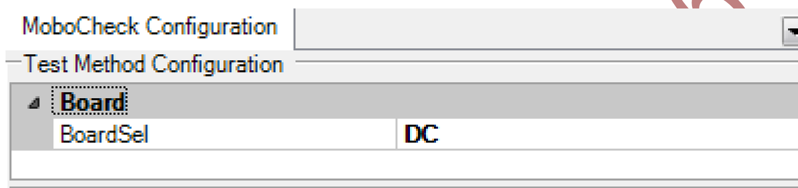
MoboCheck Test Parameters



BoardSel	Selects the board for the test. If there is only one board connected to the PC via the USB interface, the selection may be left to the default of Auto.

ReadCalResistors Test

Overview:

Read calibration board resistor values programmed into the EEPROM.

ReadCalResistors Test Parameters

There are no parameters for this test.

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Chapter 3:
Working with DC Diagnostic Library Tests

Working with Diagnostic Library6 Tests

- ✓ DC_CalDiag
- ✓ DC_RelayDiag
- ✓ HpILimitChecker
- ✓ NanoCheck
- ✓ NP_Station_Diag
- ✓ QVIcheck
- ✓ TBomb
- ✓ Test_Station_Diag
- ✓ VmeasCmrr

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Important Note:

Although the FTI 1000 system you purchased has the ability to run all the tests we provide, some of the tests are specific to the type of equipment you are using including any add on equipment. If your Focused Test representative has not covered or gone over with you specific tests that are to be run on your system(s), any excluded tests are not meant to be run and may result in run time errors..

DC_CalDiag Test

Overview:

Test integrity of Calibration board.

Requires Calibration Board to be connected.

Description:

Checks integrity of relays (open and close properly) of calibration board.

Performs a quick verification of the resistors used during calibration. Note that this check is mostly to insure the resistors are not destroyed. Resistances less than 100 Ohms are not at all accurate. Use the *DC_Resistors* in the *DC Calibration Library* for accurate resistor calibration and verification.

This test can also be used to check tester RDSon equivalent testing capability.

NOTE: This test relies mostly on the Nano VForce and ISource instruments working properly.

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DC_CalDiag Test Parameters

DC_CalDiag Configuration

Test Method Configuration

Misc	
DisconnectSense	True
ShowTBombGraph	False
Test100mOhm	False
Test10mOhm	False
Test10mOhmNeg	False
Test1mOhm	False
Test1mOhmNeg	False
Test500mOhm	False

DisconnectSense	Set True to disconnect high power instrument voltage sense. For most situations, more accuracy can be obtained by setting *DisconnectSense* to True.
ShowTBombGraph	True will display real-time resistance measurement

	results.
Test100mOhm	After calibration board relay diagnostics, use the 100mOhm resistor with a series of RDSON currents.
Test10mOhm	After calibration board relay diagnostics, use the 10mOhm resistor with a series of RDSON positive currents.
Test10mOhmNeg	After calibration board relay diagnostics, use the 10mOhm resistor with a series of RDSON negative currents.
Test1mOhm	After calibration board relay diagnostics, use the 1mOhm resistor with a series of RDSON positive currents.
Test1mOhmNeg	After calibration board relay diagnostics, use the 1mOhm resistor with a series of RDSON negative currents.
Test500mOhm	After calibration board relay diagnostics, use the 500mOhm resistor with a series of RDSON positive currents. NOTE: The calibration board must contain a revision for this test.

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DC_RelayDiag Test

Overview:

Test DC motherboard relays.

Description:

Checks integrity of relays (open and close properly) of DC motherboard.

NOTE: This test relies mostly on the Nano VForce and ISource instruments working properly.

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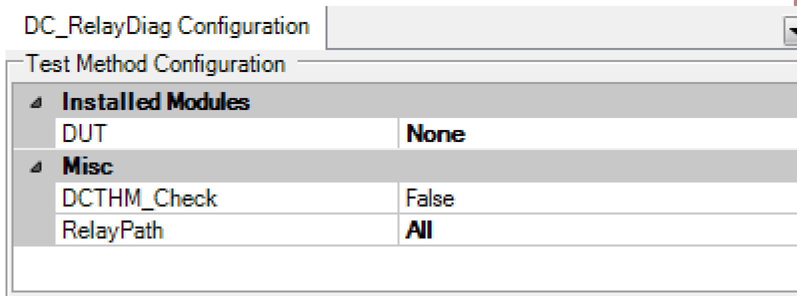
DC_RelayDiag Test Parameters



DUT	If a DUT socket is attached to the DC board banana jacks, the DUT socket Force-Sense contact can cause false relay diagnostic results. **None** – Informs the test that there is no DUT socket attached, and that all relay paths may be tested. **DUT_Socket** – Informs the test that there is a DUT socket attached, and that some relay paths cannot be tested. **CAL_Board** – Suggest not using this selection as it will not perform some relay path checks.
DCTHM_Check	True will perform additional relay check in the external Test Head MUX. NOTE: This parameter is valid only if an externalTest

	Head MUX is attached.
RelayPath	Normal relay diagnostic mode is **All**. This parameter allows selection of a specific relay path for debug purposes.

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DC_TB500mo Test

Overview:

Obsolete test. Do not use.

(This test does not utilize the latest RDSON test methodology.)

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HpILimitCheck Test

Overview:

Report maximum current High Power module is capable of providing.

Requires HP module to be installed.

HpILimitCheck Test Parameters

This test has no parameters.

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NanoCheck Test

Overview:

Performs a quick check of the Nano module VForce instrument.

Description:

Generates a series of positive and negative voltages from the VForce instrument into the high voltage measurement input.

Will also generate a series of positive and negative voltages with the VForce instrument and measure both voltage and current output via the instrument on-module voltage and current monitor circuitry.

NanoCheck Test Parameters

This test has no parameters.

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NP_Station_Diag Test

Overview:

Test relays of an external Test Station.

Test requires external N/P Test Station hardware to be attached.

Description:

Test relay integrity (properly open and close) of an external Test Station.

(NP stands for N-Channel and P-Channel.)

NP_Station_Diag Test Parameters

This test has no parameters.

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QVIcheck Test

Overview:

Quick check of QVI module VI circuitry.

This test requires a QVI module to be installed.

Description:

Generate a series of voltage and current outputs of each of the four (4) VI forcing instruments and measure the output voltage using the DC Board ADC measurement instrument.

The test will also check the VI current and voltage monitoring circuitry.

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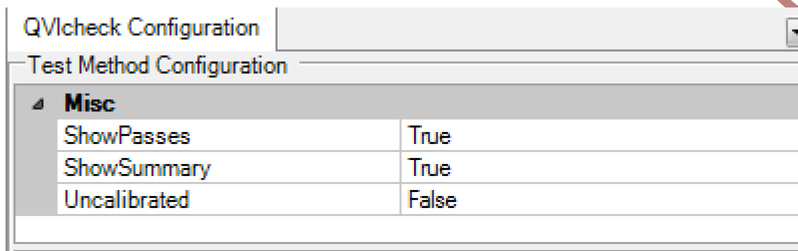
QVIcheck Test Parameters



ShowPasses	This test will generate a lot of results. True will show all test results. False will show only the failures.
ShowSummary	True will categorize each type of failure and display which VI channel failed that category.
Uncalibrated	Setting to True will widen the test limits, typically to test the functionality of a QVI module that has not yet been calibrated.

TBomb Test

Overview:

Perform the equivalent of the *RDSON* test on an external resistor.

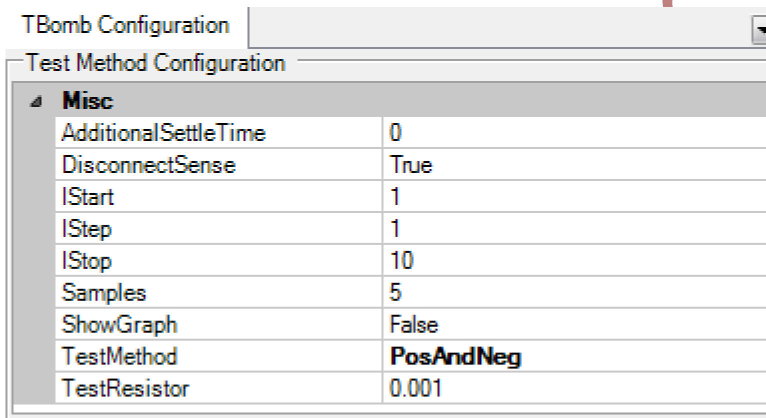
This test requires the connection of the DC Calibration board, or an external resistor.

Description:

Runs the equivalent of the *RDSON* test with a series of currents.

The advantage of this test versus the *RDSON* test using the plot tool is that this test can optionally utilize the DC Calibration board, as well as provide a graphic display overlay of both positive and negative currents.

TBombTest Parameters



AdditionalSettleTime	Ability to increase the current pulse to allow additional time for the current forcing instrument to settle.
DisconnectSense	Set True to disconnect high power instrument voltage sense. For most situations, more accuracy can be obtained by setting *DisconnectSense* to True. Some versions of the RDSON test will always disconnect the current source Sense, therefore this parameter has

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	no affect.
IStart	Specifies the starting current. This can be only a positive value.
IStep	Specifies the amount of current increase for each iteration. This can be only a positive value. Enter a value of 0 to use the same currents as the DC_CalDiag test will use.
IStop	Specifies the last current. This can be only a positive value.
Samples	Ability to change the default quantity of measurement samples that are averaged for the result. Sample rate is 11.6usec per sample. Pulse width will be automatically adjusted to accommodate extra samples.
ShowGraph	Set True to display real-time plotting graph.
TestMethod	Ability to chose positive only currents, negative only currents, or positive then negative currents used during the test.
TestResistor	Specifies the resistance used in the test. Enter the actual resistor value. It is assumed actual resistor values will never be exactly 0.001, 0.01, or 0.1. If they are, increase or decrease the value by a very small percentage, such as 0.00100001. If a calibration board is connected, the exact values of 0.001, 0.01, or 0.1 will attempt to use the calibration board resistor.

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	If desire to use an attached DC Calibration Board, enter one of the following values: 0.001, 0.01, or 0.1. The test will use the calibration board stored exact resistor value.

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Test_Station_Diag Test

Overview:

Test relays of an external Test Station.

Test requires external Test Station hardware to be attached.

Description:

Test relay integrity (properly open and close) of the external Test Station.

Test_Station_Diag Test Parameters

This test has no parameters.

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VmeasCmrr Test

Overview:

Test ADC measurement system symmetry.

Description:

The ADC measurement system has the ability to perform differential measurements. This test will force a known voltage into the positive, then into the negative inputs and shows the difference between the two inputs as a common-mode rejection ratio result.

VmeasCmrr Test Parameters

This test has no parameters.

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Chapter 4: Working with DC Calibration Library Tests

Working with DC Calibration Library 6 Tests

- ✓ DC_Digitizer
- ✓ DC_Resistors
- ✓ DVSD_Cal
- ✓ HP
- ✓ HP_Check
- ✓ HV_1200V
- ✓ HV_Force
- ✓ IF25mA_VMeas
- ✓ IF3A_VMeas
- ✓ IForce
- ✓ IForce3A
- ✓ Meter
- ✓ NanoammeterCA
- ✓ QVI_Force
- ✓ QVI_Meas
- ✓ VF10V_Cal
- ✓ VF25V_IMeas
- ✓ VForce

Important Note:

Although the FTI 1000 system you purchased has the ability to run all the tests we provide, some of the tests are specific to the type of equipment you are using including any add on equipment. If your Focused Test representative has not covered or gone over with you specific tests that are to be run on your system(s), any excluded tests are not meant to be run and may result in run time errors..

NOTE: DC calibration/verify tests will require an Agilent 34401A digital multimeter and Focused Test, Inc. calibration board to be connected to the tester.

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Recommended instrument calibration order

The reason for instrument calibration order is that some instrument calibration relies on another instrument to be properly calibrated.

Recommended calibration order:

1) DC_Resistors.
2) VForce.
3) IForce or IForce3A.
4) HV_Force (if HV module is installed).
5) Meter.
6) IF25mA_VMeas or IF3A_VMeas.
7) VF25V_IMeas.
8) NanoammeterCal.
9) VF10V_Cal.
10) HP (if HP module is installed).
11) HP_check (functional check only, valid only if HP module is installed).
12) HV_1200 (if HV module is installed, use HV for old module versions).
13) DC_Digitizer (if digitizer module is installed).
14) DVSD_Cal (if DVSD module is installed).
15) REN (if REN module is installed).
16) SCM_Cal (if SCM module is installed).
17) SOA_Cal (if SOA module is installed).
18) QVI_Force (if QVI module is installed).
19) QVI_Meas (if QVI module is installed).
20) UHV (if external UHV instrument is available).

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DC_Digitizer Test

Overview:

Calibrate or Verify Digitizer measurement instrument.

This test requires the Digitizer to be installed.

Description:

If there is no High Voltage or SCM module installed, will calibrate or verify only the 15 and 30 voltage ranges.

If a SCM module is installed and a High Voltage is not installed, will additionally calibrate or verify the 60, 100, and 200 volt ranges.

With a High Voltage module installed, will calibrate or verify all ranges.

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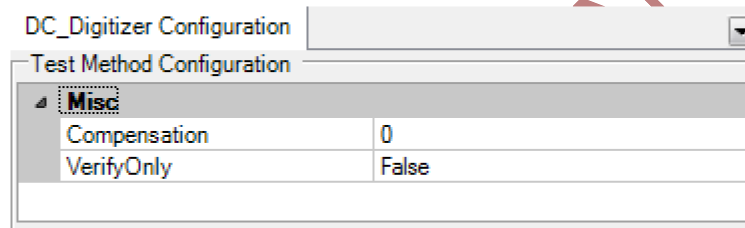
DC_Digitizer Parameters



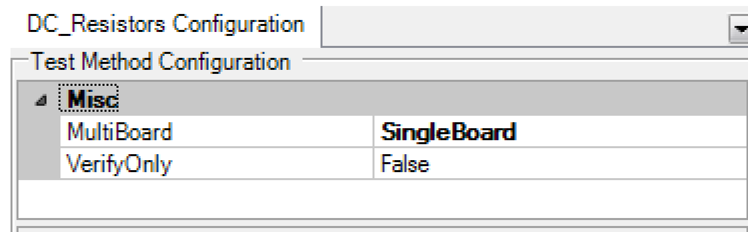
Compensation	Parameter is not used.
VerifyOnly	Set True to verify Digitizer instrument calibration, False to calibrate the Digitizer instrument.

DC_Resistors Test

Overview:

Calibrate or Verify calibration board resistors used during tester instrument calibration.

DC_Resistors Parameters



MultiBoard	**SingleBoard** is the typical setting. Use **CalVfyBoard2** if the calibration board is connected to DCBoard2 (Resource TAB) and wish to calibrate or verify the calibration board with DCBoard (Resource TAB).
VerifyOnly	Set True to verify Digitizer instrument calibration, False to calibrate the Digitizer instrument.

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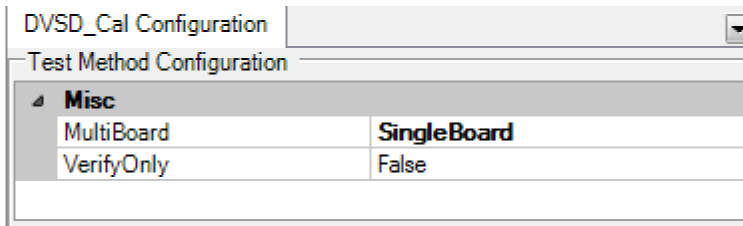
DVSD_Cal Test

Overview:

Calibrate or Verify DVSD instrument.

The test requires a DVSD module to be installed.

DVSD_Cal Parameters



MultiBoard	**SingleBoard** is the typical setting. Use **CalVfyBoard2** if the calibration board is connected to DCBoard2 (Resource TAB) and wish to calibrate or verify the calibration board with DCBoard (Resource TAB).
VerifyOnly	Set True to verify Digitizer instrument calibration, False to calibrate the Digitizer instrument.

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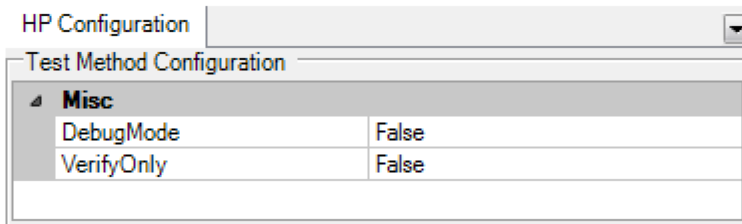
HP Test

Overview:

Calibrate or Verify High Power instrument.

The test requires a High Power module to be installed.

HP Parameters



DebugMode	True will use only one (1) ADC sample per pulse, as well as perform current limit checking. False is the normal calibration or verify mode.
VerifyOnly	Set True to verify Digitizer instrument calibration, False to calibrate the Digitizer instrument.

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HP_check Test

Overview:

Check High Power instrument functionality.

The test requires a High Power module to be installed.

Description:

The test checks capacitor bank voltage settings, current limits, voltage compliance, and settling time.

HP_check Parameters

This test does not have any parameters.

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HV Test

Overview:

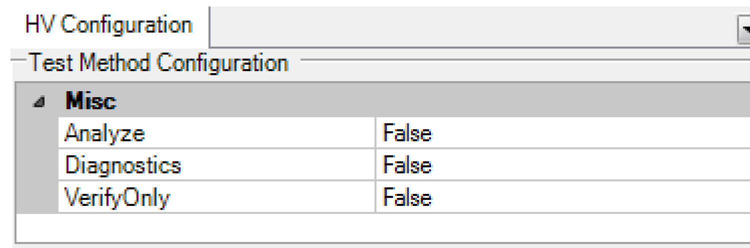
Calibrate or Verify High Voltage instrument.

This test requires the 800V High Voltage instrument to be installed.

Description:

There are different versions of the High Voltage instrument. This test calibrates and/or verifies the 800V version.

HV Parameters



Analyze	Parameter is not used.
Diagnostics	Set True to calibrate and/or verify High Voltage capacitor bank programming. NOTE that the accuracy of the capacitor bank voltage setting does not affect test accuracy, such as BVDSS, etc. Most tests set the capacitor bank voltage to at least 150V greater than the test requires. The calibration of the capacitor bank is only necessary to insure that the capacitor voltage closely matches the desired programmed voltage. When *Diagnostics* is set to True, will also perform high voltage and current extreme checks of the High Voltage module.
VerifyOnly	Set True to verify High Voltage instrument calibration,

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	False to calibrate the High Voltage instrument.

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HV_1200V Test

Overview:

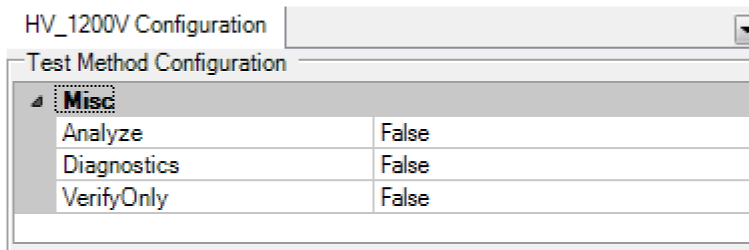
Calibrate or Verify High Voltage instrument.

This test requires the 1200V High Voltage instrument to be installed.

Description:

There are different versions of the High Voltage instrument. This test calibrates and/or verifies the 1200V version.

HV_1200V Parameters



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Analyze	Parameter is not used.
Diagnostics	Set True to calibrate and/or verify High Voltage capacitor bank programming. NOTE that the accuracy of the capacitor bank voltage setting does not affect test accuracy, such as BVDSS, etc. Most tests set the capacitor bank voltage to at least 150V greater than the test requires. The calibration of the capacitor bank is only necessary to insure that the capacitor voltage closely matches the desired programmed voltage. When *Diagnostics* is set to True, will also perform high voltage and current extreme checks of the High Voltage module.
VerifyOnly	Set True to verify High Voltage instrument calibration,

	False to calibrate the High Voltage instrument.

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HV_Force Test

Overview:

Calibrate or Verify High Voltage instrument.

This test requires a High Voltage instrument to be installed.

Description:

This test calibrates only the voltage forcing portion of the High Voltage instrument. To fully calibrate the High Voltage instrument, use the HV or HV_1200V test.

HV_Force Parameters

HV_VForce Configuration	
Test Method Configuration	
Misc	
VerifyOnly	False

VerifyOnly	Set True to verify High Voltage instrument calibration, False to calibrate the High Voltage instrument.

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IF25mA_VMeas Test

Overview:

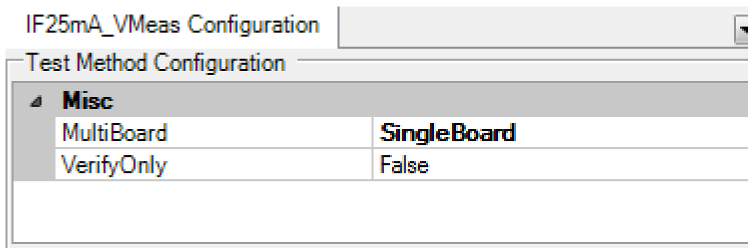
Calibrate or Verify Nano module current source instrument.

This test requires the standard Nano (with 25mA ISource) instrument to be installed.

Description:

There are different versions of the Nano module current source instrument. This test calibrates and/or verifies the 25mA ISource version voltage measurement circuitry.

IF25mA_VMeas Parameters



MultiBoard	**SingleBoard** is the typical setting. Use **CalVfyBoard2** if the calibration board is connected to DCBoard2 (Resource TAB) and wish to calibrate or verify the calibration board with DCBoard (Resource TAB).
VerifyOnly	Set True to verify High Voltage instrument calibration, False to calibrate the High Voltage instrument.

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IF3A_VMeas Test

Overview:

Calibrate or Verify Nano module current source instrument.

This test requires the NanoB (with 3A ISource) instrument to be installed.

Description:

There are different versions of the Nano module current source instrument. This test calibrates and/or verifies the 3A ISource version voltage measurement circuitry.

IF3A_VMeas Parameters

IF3A_VMeas Configuration

Test Method Configuration

Misc

VerifyOnly False

VerifyOnly	Set True to verify High Voltage instrument calibration, False to calibrate the High Voltage instrument.

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IForce Test

Overview:

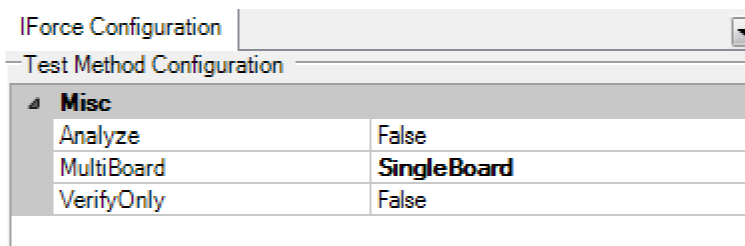
Calibrate or Verify the Nano module current source instrument.

The test requires the standard Nano module with 25mA current source to be installed.

Description:

There are different versions of the Nano module current source instrument. This test calibrates and/or verifies the 25mA ISource version.

IForce Parameters



Analyze	Set True to enable additional current source verification levels. Sometimes this can aid in failure repair. False is the normal calibration/verify mode.
MultiBoard	**SingleBoard** is the typical setting. Use **CalVfyBoard2** if the calibration board is connected to DCBoard2 (Resource TAB) and wish to calibrate or verify the calibration board with DCBoard (Resource TAB).
VerifyOnly	Set True to verify Digitizer instrument calibration, False to calibrate the Digitizer instrument.

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IForce 3A Test

Overview:

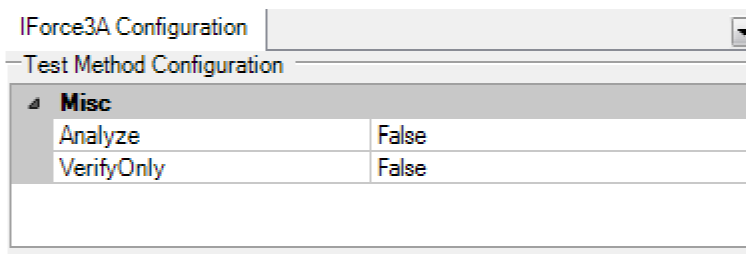
Calibrate or Verify the Nano module current source instrument.

The test requires the NanoB module with 3A current source to be installed.

Description:

There are different versions of the Nano module current source instrument. This test calibrates and/or verifies the 3A ISource version.

IForce3A Parameters



Analyze	Set True to enable additional current source verification levels. Sometimes this can aid in failure repair. False is the normal calibration/verify mode.
VerifyOnly	Set True to verify Digitizer instrument calibration, False to calibrate the Digitizer instrument.

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Meter Test

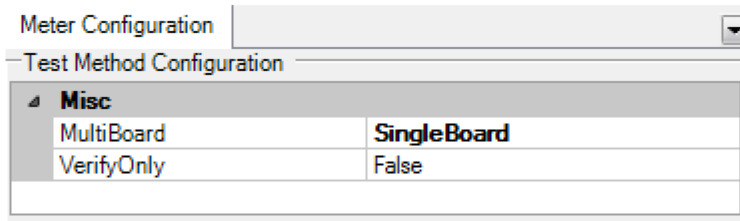
Overview:

Calibrate or Verify the ADC measurement instrument.

The test requires a minimum of Nano or NanoB module to be installed.

Requires the High Voltage (HV) module to be installed in order to calibrate/verify the Meter input ranges of 100V and greater.

Meter Parameters



MultiBoard	**SingleBoard** is the typical setting. Use **CalVfyBoard2** if the calibration board is connected to DCBoard2 (Resource TAB) and wish to calibrate or verify the calibration board with DCBoard (Resource TAB).
VerifyOnly	Set True to verify Digitizer instrument calibration, False to calibrate the Digitizer instrument.

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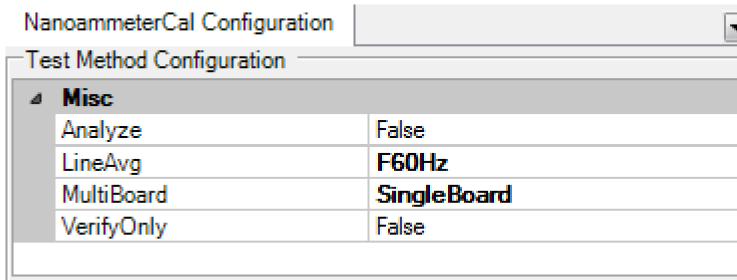
NanoammeterCal Test

Overview:

Calibrate or Verify the Nano module current measurement instrument.

The test requires the Nano or NanoB module to be installed.

NanoammeterCal Parameters



Analyze	Set True to enable additional current setting verification levels. Sometimes this can aid in failure repair. False is the normal calibration/verify mode.
LineAvg	Must be set to 50Hz or 60Hz, depending on AC line power source.
MultiBoard	**SingleBoard** is the typical setting. Use **CalVfyBoard2** if the calibration board is connected to DCBoard2 (Resource TAB) and wish to calibrate or verify the calibration board with DCBoard (Resource TAB).
VerifyOnly	Set True to verify Digitizer instrument calibration, False to calibrate the Digitizer instrument.

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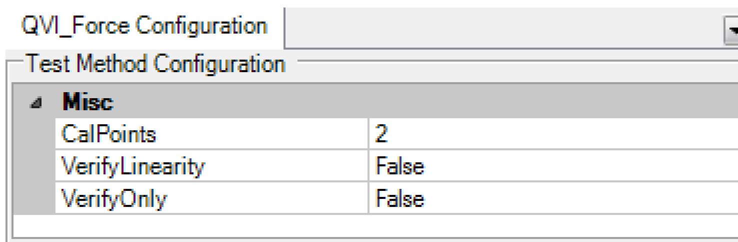
QVI_Force Test

Overview:

Calibrate or Verify the QVI module current and voltage sourcing instruments.

The test requires the QVI module to be installed.

QVI Force Parameters



CalPoints	Defines the quantity of points to use to determine gain and offset slope. Default is 2.
VerifyLinearity	Set True to verify 10 points per range. Default is False, which will verify only full scale and 1% levels of range.
VerifyOnly	Set True to verify Digitizer instrument calibration, False to calibrate the Digitizer instrument.

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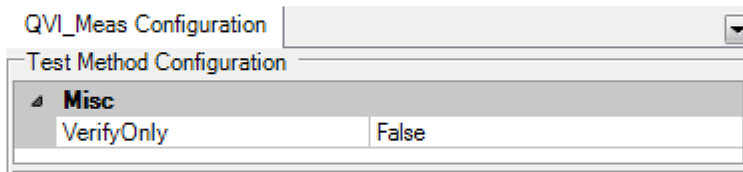
QVI_Meas Test

Overview:

Calibrate or Verify the QVI module current and voltage measurement instruments.

The test requires the QVI module to be installed.

QVI_Meas Parameters



VerifyOnly	Set True to verify Digitizer instrument calibration, False to calibrate the Digitizer instrument.

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REN Test

Overview:

Calibrate or Verify the REN (Reverse Energy) module instruments.

The test requires the REN module to be installed.

REN Parameters

REN_cal Configuration

Test Method Configuration

Misc

VerifyOnly	False

VerifyOnly	Set True to verify Digitizer instrument calibration, False to calibrate the Digitizer instrument.

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SCM Test

Overview:

Calibrate or Verify the SCM (Surge Current) module instruments.

The test requires the SCM module to be installed.

SCM Parameters

SCM_Cal Configuration

Test Method Configuration

Misc	
VerifyOnly	False

VerifyOnly	Set True to verify Digitizer instrument calibration, False to calibrate the Digitizer instrument.

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SOA Test

Overview:

Calibrate or Verify the SOA (Safe Operating Area) module instruments.

The test requires the SOA module to be installed.

SOA Parameters

SOA_Cal Configuration

Test Method Configuration

Misc

VerifyOnly	False

VerifyOnly	Set True to verify Digitizer instrument calibration, False to calibrate the Digitizer instrument.

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UHV Test

Overview:

Calibrate or Verify the UHV (Ultra-High Voltage) module instruments.

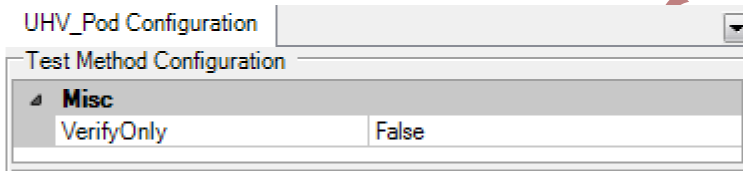
The test requires the UHV module.

Description:

The UHV ribbon cable must be connected to the tester ILT port.

The DS-OUT banana jack of the UHV box (labeled DFOUT on the PCB) must be connected to +DMM. The DS-TESTER banana jack of the UHV box (labeled as DFIN on the PCB) must be connected to –DMM.

UHV Parameters



VerifyOnly	Set True to verify Digitizer instrument calibration, False to calibrate the Digitizer instrument.

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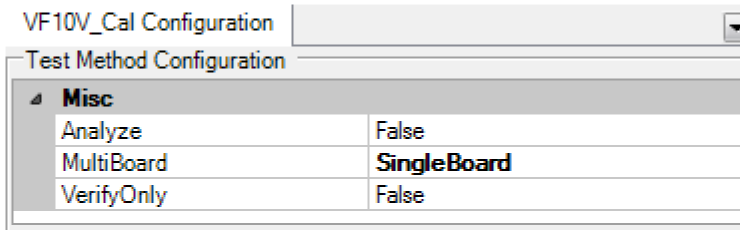
VF10V_Cal Test

Overview:

Calibrate or Verify the Nano module 10V voltage source instrument.

The test requires the Nano or NanoB module to be installed.

VF10V_Cal Parameters



Analyze	Set True to enable additional voltage source verification levels. Sometimes this can aid in failure repair. False is the normal calibration/verify mode.
MultiBoard	**SingleBoard** is the typical setting. Use **CalVfyBoard2** if the calibration board is connected to DCBoard2 (Resource TAB) and wish to calibrate or verify the calibration board with DCBoard (Resource TAB).
VerifyOnly	Set True to verify Digitizer instrument calibration, False to calibrate the Digitizer instrument.

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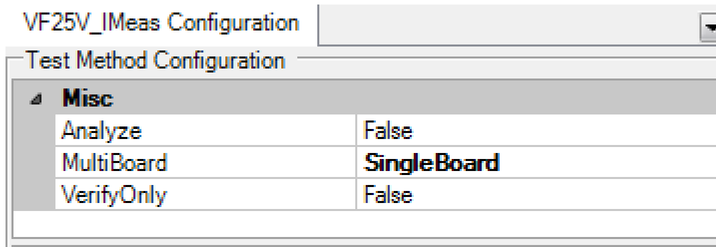
VF25V_Imeas Test

Overview:

Calibrate or Verify the Nano module VForce current measurement circuitry.

The test requires the Nano or NanoB module to be installed.

VF25V_Imeas Parameters



Analyze	Set True to enable additional voltage source verification levels. Sometimes this can aid in failure repair. False is the normal calibration/verify mode.
MultiBoard	**SingleBoard** is the typical setting. Use **CalVfyBoard2** if the calibration board is connected to DCBoard2 (Resource TAB) and wish to calibrate or verify the calibration board with DCBoard (Resource TAB).
VerifyOnly	Set True to verify Digitizer instrument calibration, False to calibrate the Digitizer instrument.

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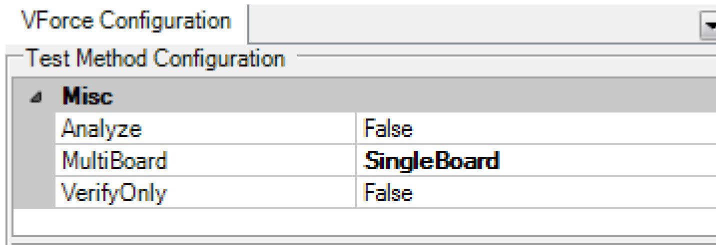
VForce Test

Overview:

Calibrate or Verify the Nano module VForce instrument output.

The test requires the Nano or NanoB module to be installed.

VForce Parameters



Analyze	Set True to enable additional voltage source verification levels. Sometimes this can aid in failure repair. False is the normal calibration/verify mode.
MultiBoard	**SingleBoard** is the typical setting. Use **CalVfyBoard2** if the calibration board is connected to DCBoard2 (Resource TAB) and wish to calibrate or verify the calibration board with DCBoard (Resource TAB).
VerifyOnly	Set True to verify Digitizer instrument calibration, False to calibrate the Digitizer instrument.

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Chapter 5: Maintenance Part A

System Configuration/Test System Configuration/Calibration

- ✓ Motherboard/Module Block Diagram
- ✓ Main Connect Block Diagram
- ✓ Measurement Block Diagram
- ✓ Motherboard Specifications
- ✓ FTI 1000 Calibration
- ✓ FTI UHV Pod Calibration

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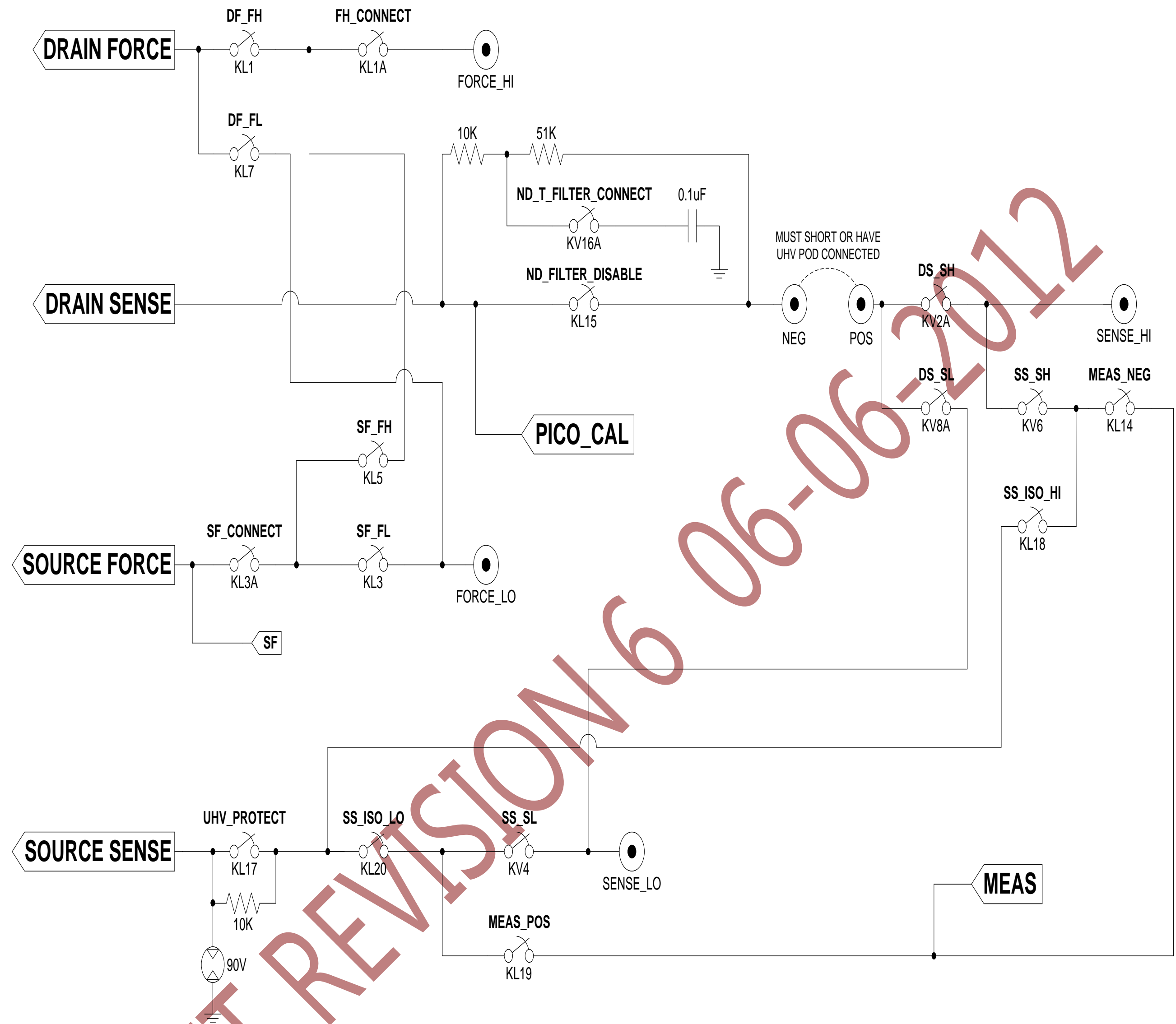
System and Test System Configuration and Calibration

Motherboard/Module Block Diagram

Main Connect Block Diagram



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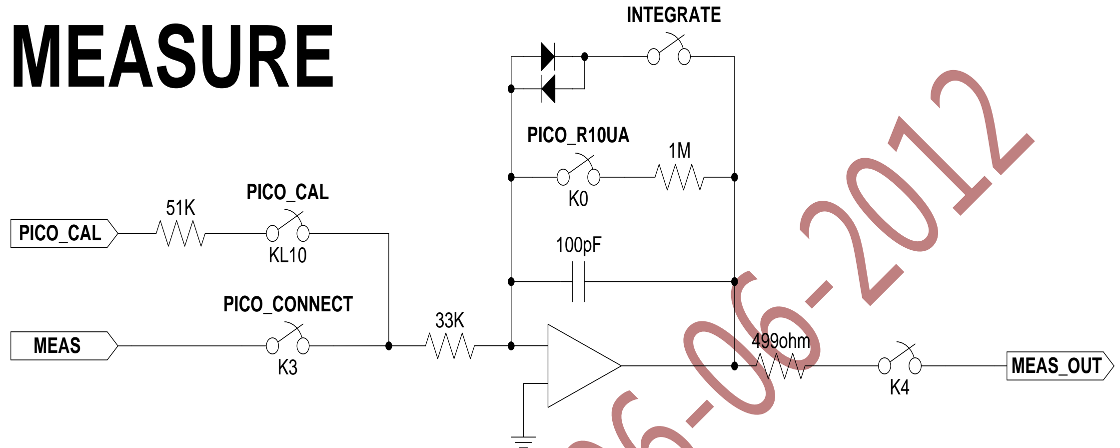
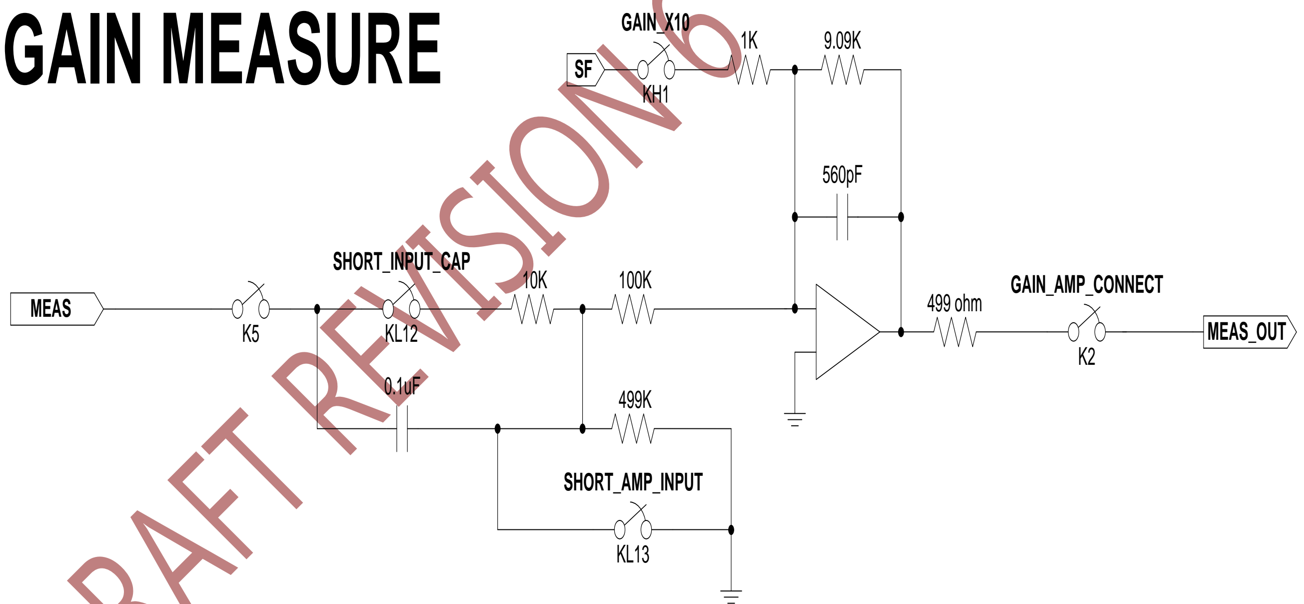
Measurement Block Diagram





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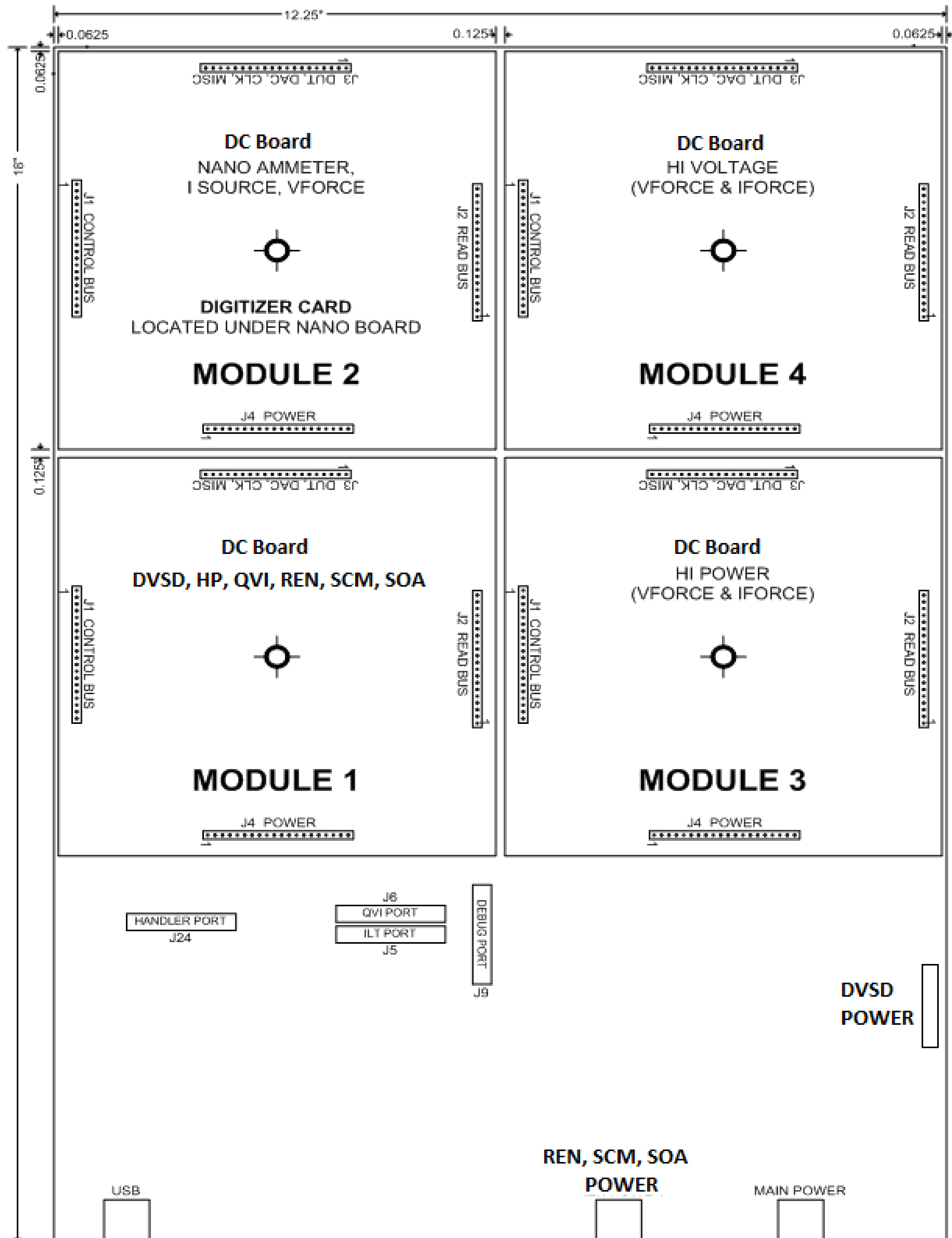
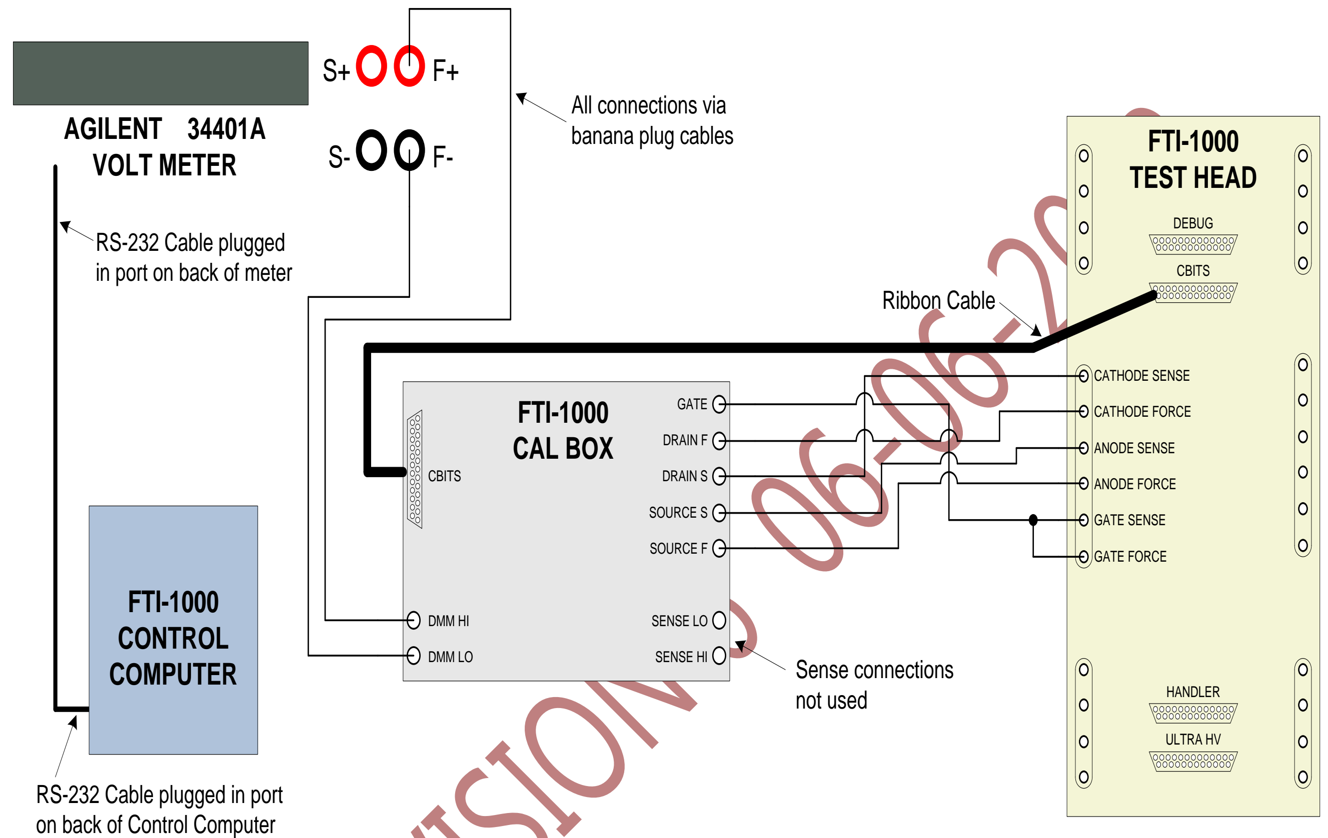
Motherboard Specifications FT 1000



FTI 1000 Calibration



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FTI 1000 UHV POD Calibration

FTI-1000
TEST HEAD
DEBUG
CBITS

AGILENT 34401A
VOLT METER
S+ F+
S- F-

All connections via
banana plug cables

RS-232 Cable plugged
in port on back of meter

CATHODE SENSE
CATHODE FORCE
ANODE SENSE
ANODE FORCE
GATE SENSE
GATE FORCE

Ribbon Cable

FTI-1000
CONTROL
COMPUTER

FTI-1000
UHV POD
HIGH VOLTAGE SOURCE
DRAIN F OUT
DRAIN F IN
DRAIN S OUT
DRAIN S IN
UHV

HANDLER
UHV

RS-232 Cable plugged in port
on back of Control Computer

USB

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Chapter 6: Maintenance Part B

Motherboard Relay Check Loops

The relay paths that are tested are dependent on the hardware revision and modules that are installed. Attempting to show each combination will cause confusion and would most likely be out of date. Therefore, it is suggested to use the relay graphical display GUI to view specific relay paths.

To view particular relay paths, select the desired loop in the *RelayPath* user parameter of the *DC_RelayDiag* test and monitor the relay graphic display while the test is ran. Note that it is possible to step through each relay state change using the relay graphic display.

Refer to Appendices A for a method to debug relay failures using the relay graphic display.

The following picture is an example of one of the relay check loops. It shows a number of relays closed and red trace showing the connection path between relays and instruments. For this example, the NANO VFORCE is the voltage source that applies a voltage through the highlighted relay paths to the VMEAS instrument which will measure a voltage if all relays close properly, and no voltage if any relay is open.

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(Example of loop 1 relay path.)

The above relay graphic example also indicates what instruments are installed: HV, HP, DVSD, and NANO modules. The VMEAS is part of the DC motherboard, therefore will always be installed.

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Chapter 7: DC Instrument Specifications

DC Instrument Specifications

- ✓ Meter
- ✓ IF50V25MA
- ✓ VF50V100MA
- ✓ VF55V100A
- ✓ IF55V100A
- ✓ VF10V
- ✓ VF800V100MA
- ✓ IF800V100MA

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Meter

Low V Ranges

100mV Range	Accuracy 0.1% of Value +/- 1mV
1V Range	Accuracy 0.1% of Value +/- 1mV
10V Range	Accuracy 0.1% of Value +/- 4mV

High V Ranges

10V Range	Accuracy 0.2% of Value +/- 40mV
20V Range	Accuracy 0.2% of Value +/- 40mV
100V Range	Accuracy 0.2% of Value +/- 40mV
200V Range	Accuracy 0.2% of Value +/- 80mV
800V Range	Accuracy 0.2% of Value +/- 400mV

IF50V25MA (Max Voltage = +/-40V, Current = +/-25mA)

Current Forcing Ranges

Range	Accuracy
2.5uA Range	Accuracy 0.1% of Value +/- 10nA
25uA Range	Accuracy 0.1% of Value +/- 100nA
250uA Range	Accuracy 0.1% of Value +/- 1uA
2.5mA Range	Accuracy 0.1% of Value +/- 10uA
25mA Range	Accuracy 0.1% of Value +/- 100uA

Voltage Measurement

Meter Voltage input selection up to +/- 10V
Full scale using meter Monitor_IF25MA_Voltage input selection
Full scale Accuracy 0.1% of Value +/- 1mV, +/- 20mV @ 0mA

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VF50V100MA (Max Voltage = +/-40V, Current = +/-100mA)

Voltage Forcing Ranges

1V Range	Accuracy 0.1% of Value +/- 1mV
2V Range	Accuracy 0.1% of Value +/- 2mV
5V Range	Accuracy 0.1% of Value +/- 5mV
10 V Range	Accuracy 0.1% of Value +/- 10mV
20 V Range	Accuracy 0.1% of Value +/- 20mV
50V Range	Accuracy 0.1% of Value +/- 50mV

Current Measurement Ranges (Meter input selection = Monitor_VF50V_Current)

100nA Range	Accuracy 0.1% of Value +/- 2nA
1uA Range	Accuracy 0.1% of Value +/- 5nA
10uA Range	Accuracy 0.1% of Value +/- 40nA
100uA Range	Accuracy 0.1% of Value +/- 400nA
1mA Range	Accuracy 0.25% of Value +/- 4uA
10mA Range	Accuracy 0.25% of Value +/- 40uA
100mA Range	Accuracy 0.25% of Value +/- 400uA

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VF55V100A (Max Voltage = 55V, Current = 100A, VA = 3000VA)

Voltage Forcing Ranges

10V Range	Accuracy 0.1% of Value +/- 50mVeah
100V Range	Accuracy 0.1% of Value +/- 500mV

Current Measurement Ranges (Meter input selection = Monitor_60V100A_Current)

100mA Range	Accuracy 0.25% of Value +/- 0.25mA
1A Range	Accuracy 0.25% of Value +/- 2.5mA
10A Range	Accuracy 0.25% of Value +/- 25mA
100A Range	Accuracy 0.25% of Value +/- 250mA

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IF55V100A (Max Voltage = 55V, Current = 100A, VA = 3000VA)

Current Forcing Ranges

100mA Range	Accuracy 0.25% of Value +/- 0.25mA
1A Range	Accuracy 0.25% of Value +/- 2.5mA
10A Range	Accuracy 0.25% of Value +/- 25mA
100A Range	Accuracy 0.25% of Value +/- 250mA

Voltage Measurement Ranges (Meter input selection = Monitor_60V100A_Voltage)

10V Range	Accuracy 0.1% of Value +/- 50mV
100V Range	Accuracy 0.1% of Value +/- 500mV

VF10V (Max Voltage = +/-10V, Current = +/-5mA)

Current Range Selections (IDS from VF50V100MA)

1mA Range	Accuracy 0.25% of Value +/- 1uA
10mA Range	Accuracy 0.25% of Value +/- 10uA
100mA Range	Accuracy 0.25% of Value +/- 100uA

Voltage Forcing Ranges

10V	Accuracy (0.1% of Value +/- 10mV

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VF800V100MA (Max Voltage=+/-800V, Current=+/-100mA, VA=70V)

(Unregulated Power supply voltage control 0 1000V)

Voltage Forcing Ranges

50V Range	Accuracy 0.2% of Value +/- 50mV
100V Range	Accuracy 0.2% of Value +/- 100mV
200V Range	Accuracy 0.2% of Value +/- 200mV
500V Range	Accuracy 0.2% of Value +/- 500mV
1000V Range	Accuracy 0.2% of Value +/- 1V

Current Measurement Ranges (Meter input selection = Monitor_800V100MA_Current)

10uA Range	Accuracy 0.5% of Value +/- 0.4uA
100uA Range	Accuracy 0.4% of Value +/- 0.3uA
1mA Range	Accuracy 0.4% of Value +/- 1.5uA
10mA Range	Accuracy 0.25% of Value +/- 3uA
100mA Range	Accuracy 0.25% of Value +/- 50uA

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IF800V100MA (Max Voltage +/-800V, Current =+/-100mA, VA=70VA)

(Unregulated Power supply voltage control 0 1000V)

Current Forcing Ranges

10uA Range	Accuracy 0.5% of Value +/- 0.4uA
100uA Range	Accuracy 0.4% of Value +/- 0.3uA
1mA Range	Accuracy 0.4% of Value +/- 1.5uA
10mA Range	Accuracy 0.25% of Value +/- 15uA
100mA Range	Accuracy 0.25% of Value +/- 150uA

Voltage Measurement Ranges (Meter input selection = Monitor_800V100MA_Voltage)

50V Range	Accuracy 0.2% of Value +/- 20mV
100V Range	Accuracy 0.2% of Value +/- 40mV
200V Range	Accuracy 0.2% of Value +/- 80mV
500V Range	Accuracy 0.2% of Value +/- 200mV
1000V Range	Accuracy 0.2% of Value +/- 400mV

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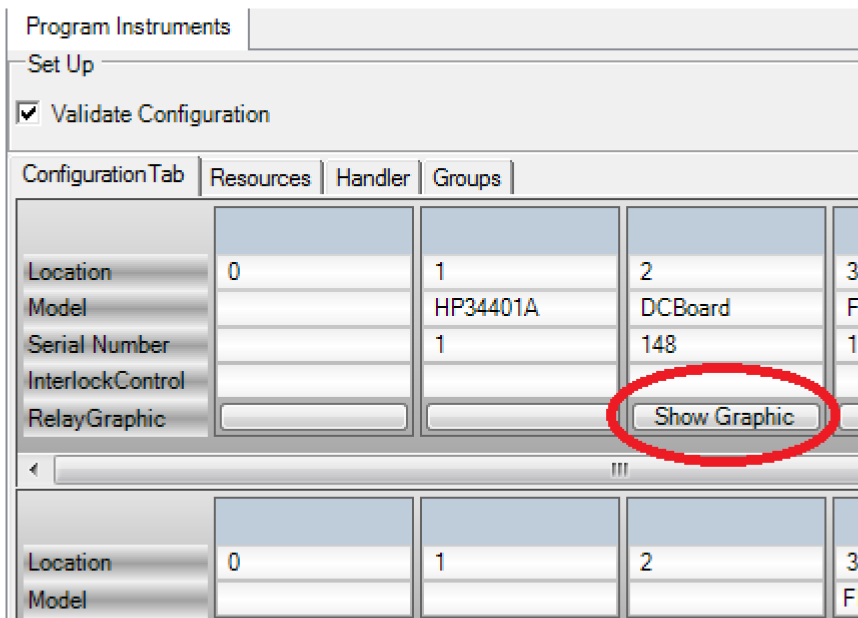
Appendices A:

Invoking the Relay Graphic Display

To invoke the relay graphic, go to the *Program Instruments* TAB. On that TAB, select the *Configuration Tab* TAB. On the *Configuration Tab* TAB, go to the column with the appropriate DC Board, and press the *Show Graphic* button (shown below).



NOTE: The *Show Graphic* button is enabled only if the board was detected when the test program was loaded.

The graphic display of other external hardware, such as Calibration Box, is displayed only after running a test at least one time, prior to pressing the *Show Graphic* button. The test must use the external hardware during the test.

The *Show Graphic* button may be pressed subsequent times if desired, even though a relay graphic is already displayed.

Active paths will be shown with a red trace and green relay contacts. If there is nothing active, that indicates the next relay state change will be all relays opened.

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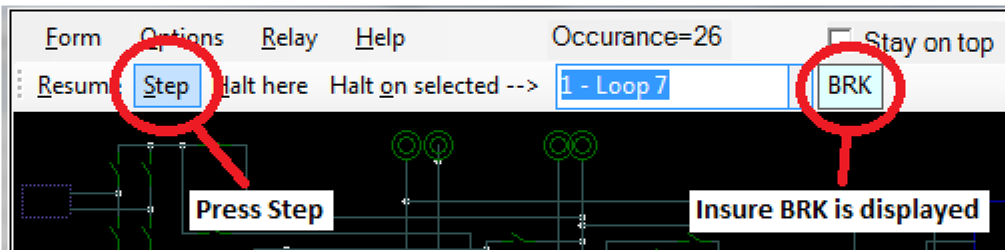
Control Buttons

Resume

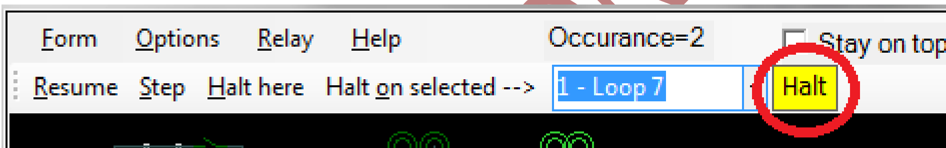
Clear break point, and if test execution is halted as shown by the *Halt* status indicator, resume from halt state.

Step

Allow manual stepping to each relay state change. If a test is not executing, pressing *Step* will enable test execution halt on the first relay state change of the test.



If the test is halted as shown by the *Halt* status indicator, pressing Step will run the test to the next relay state change.



When halted, the graphical display will show what the relay state will be, not what the relay state is. The reason for this is to allow the relay state(s) to be modified prior to execution.

Halt here

The Halt here button is a means to cause test execution to always halt at the present state.

The *Halt here* button can be used only if the test is already halted, typically by the *Step* button. After the test is paused, pressing *Halt here* will allow the test to run to completion. When the test is ran a subsequent time, the test will run to the same stated from which the *Halt here* button was previously pressed.

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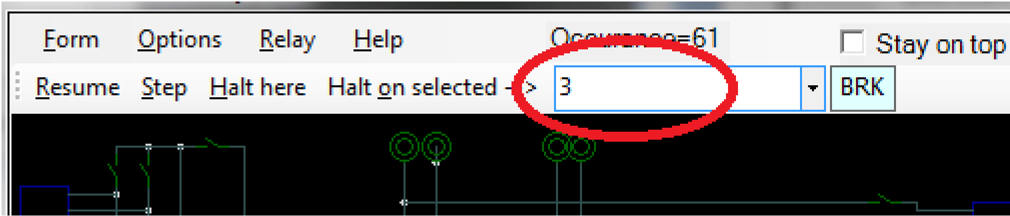
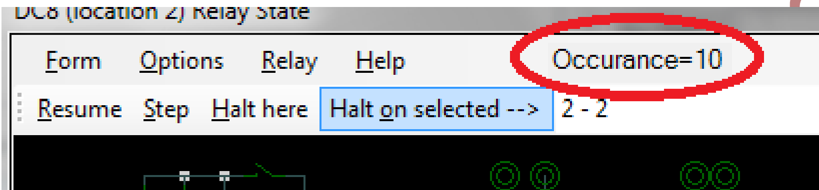
Halt on selected

After a test has run at least one time, it is possible to enter a relay state occurrence number, or select from the combo-box list, to halt on. Type the number in the combo-box as shown below. After the number has been entered, press the Halt on selected button and insure the BRK status is indicated as shown below.



When stepping through each relay state change, there is an occurrence number displayed, as shown below. The occurrence number will increment with each step.



When the test has halted, press the *Halt on selected* button to resume the test. If the relay state occurrence of the halted state is less than the defined *Halt on selected* occurrence number, the test will run to the specified relay state occurrence and then halt. If the relay state occurrence is greater than or equal to the specified *Halt on selected* occurrence number, the test will run to completion, and then halt on the specified occurrence number the next time the test is ran.

Form menu items

Refresh

Update or refresh the relay graphic display.

Page Setup

Configure the relay graphic printing, or saving to file, format. This defines Landscape or Portrait style as well as the borders.

Print

Print the relay graphic display to printer.

Print to File (Color)

Print the relay graphic display to a color picture file.

Print to File (B/W)

Print the relay graphic display to a black and white picture file.

Copy relay config info to clibpboard

This menu item copies a list relays that are not associated with the graphic relays, and a list of relays in the graphic that are not associated with a physical relay, to be copied to the clipboard for pasting into a text editor or document.

This menu item is primarily for driver code development purposes.

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Close

Close the relay graphic display.

The display can be invoked again by the *Show Graphic* button on the *Configuration Tab* TAB of FTI Studio.

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Options menu items

Update on all state changes

When this menu item is checked, allows the graphic to update the relay state and highlight appropriate signal paths each time the relay state changes. When unchecked, the graphic display will be updated only when halted.

Note that when updating the graphic with each relay state change will make the test run slower.

Allow to change relay

When this menu item is checked, double-clicking on a relay will allow the graphic to change the relay state.

If the *Relay state takes effect immediately* is not checked, the relay state will not take effect until the test is resumed.

Relay state takes effect immediately

When checked, and if *Allow to change relay* menu item is checked, double-clicking on a relay will set ALL relays to the displayed state.

WARNING! It is possible to damage the hardware instruments, DUT, or relay if this mode is enabled. Use extreme caution.

Halt on all errors

When checked, will halt test execution on the next relay state change if an error occurred. Note that when halted, the relay graphic display shows what the new state of the relays will be, not the state in which the error occurred.

A test must be designed with the *GraphicTagError* function call in order for this feature to be utilized. Note that most tests are not designed with this function call.

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Halt on first error

When checked, will halt test execution on the next relay state change after the first error occurrence in the test. Note that when halted, the relay graphic display shows what the new state of the relays will be, not the state in which the error occurred.

A test must be designed with the *GraphicTagError* function call in order for this feature to be utilized. Note that most tests are not designed with this function call.

Stay on top

When checked, or when the *Stay on top* check box is checked, will keep the relay graphic display form on top of other forms.

Caution: Make sure the relay graphic display form is closed, or the *Stay on top* is unchecked prior to closing a test program, or closing the FTI Studio application. With *Stay on top* checked, it is possible that the form will hide a FTI Studio dialog box which may require a response in order to continue.

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Relay menu items

Open all relays

As the name implies, open all relays. If the Options menu item *Relay state takes effect immediately* is not checked, the relays will not open until test execution is continued.

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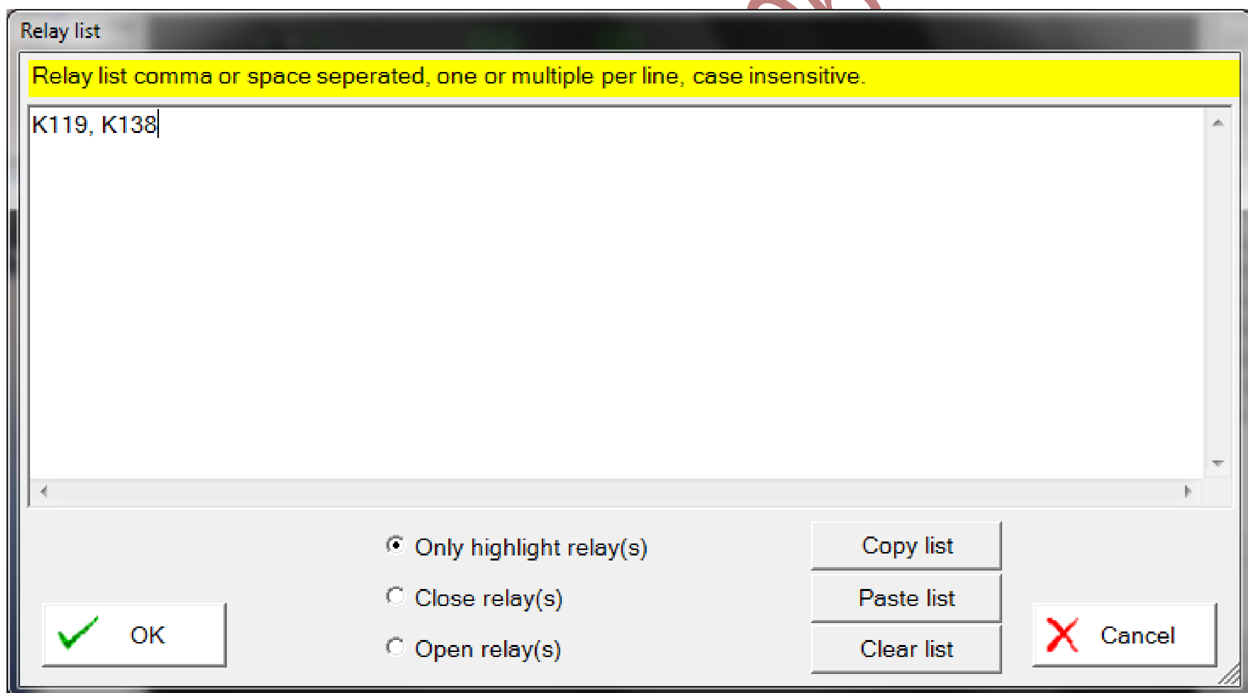
Select relays

Bring up a dialog box in which relay numbers may be entered in order to highlight, open, or close the specified relays.



Unselect relay(s)

If any relays are highlighted, this menu item will remove the highlighting. This action will not change the state of relays.

Select Relay Error State

This menu item allows the selection of a relay state associated with an error condition.

NOTE: The error selection may not be a correct representation of the relay state displayed. It is important to note that in order to properly associate an error with a relay state display, the test function must be written in segments in which a single relay configuration is executed and the error condition analyzed and notified prior to setting up a new relay configuration.

For the relay state to take effect, the *Relay state takes effect immediately* option must be checked. Double-click on any relay to change its state. (Double-click again to change it back.) That will also update all the other relays.

Copy relay(s) to clipboard

Creates a text definition of relays to close and copy to the clipboard. That text then may be pasted into a text file such as Notepad, or Visual Studio when creating a test.

This methodology allows one to select the desired relays and paste the relay definition directly into source code when creating a test.

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Appendices B:

Debugging relay failure using the Relay Graphic Display

Another useful purpose of the relay graphic display is to debug and identify relay failures. Refer to Appendices A for the methodology to invoke the relay graphic.

The *Allow to change relay* and *Relay state change takes effect immediately* Options menu items must be checked.

When not running a test or a test is not halted, select a relay path from one tester banana jack to another by double-clicking the appropriate relays. Connect an Ohmmeter between the appropriate banana jacks as shown in the example below.

One-by-one, open, then close a relay in the path by double-clicking on the relay. With a relay open, the Ohmmeter should read infinite Ohms, or an open. With the relay closed, the Ohmmeter should read near zero (0) Ohms.

For example, with KH112 and KH9 in the above example closed, the Ohmmeter should read near zero Ohms. Double-click KH112 to open the relay should show an open on the Ohmmeter. Double-click KH112 again should show a short on the Ohmmeter.

Do the same with KH9 to insure that relay will open and close.

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